

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J43 MLB SCHEMATIC DVT

REV 6.5.0

4/09/13

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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ALIASES RESOLVED

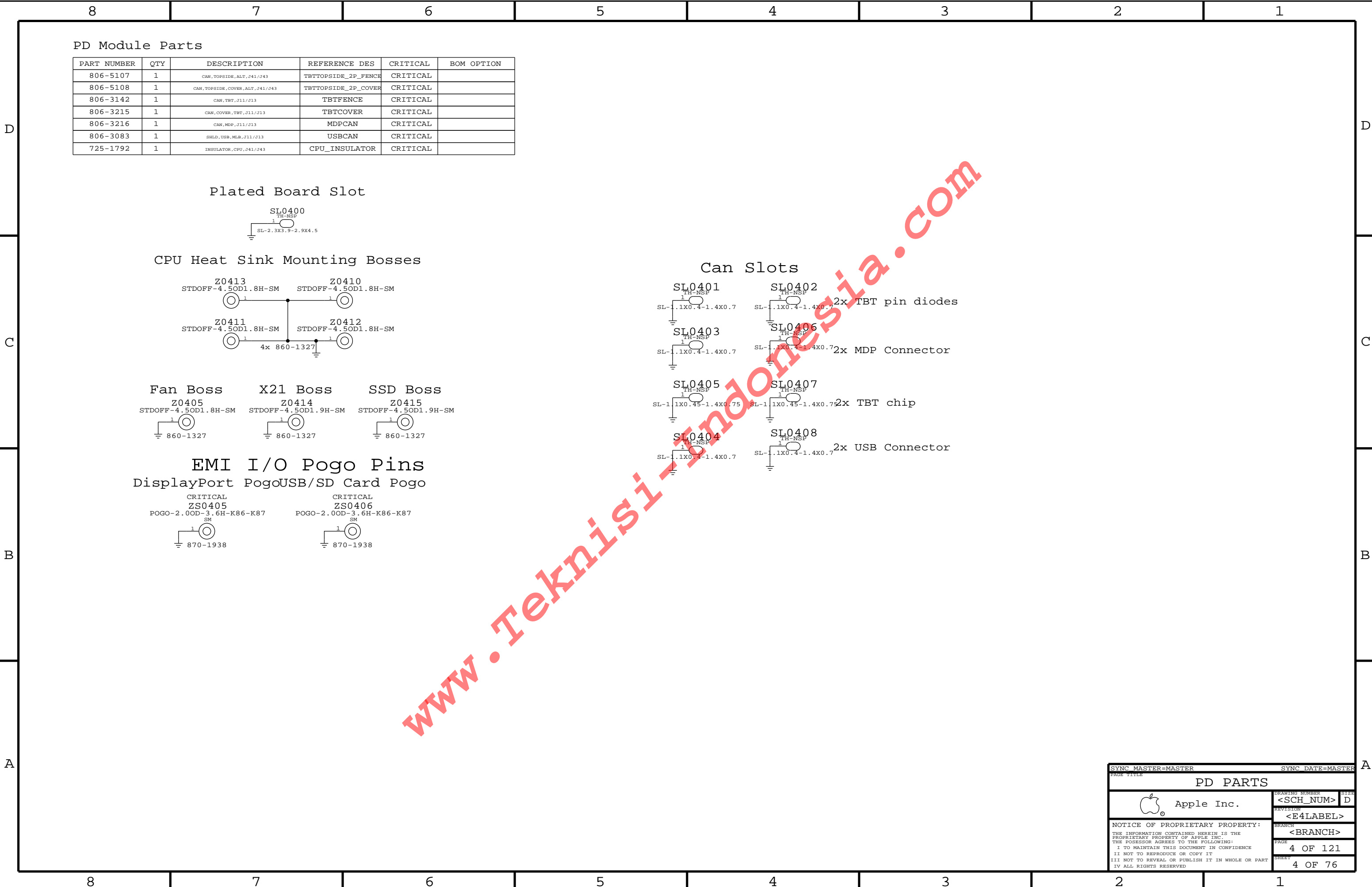
Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9800	1	SCHEM,MLB,J43	SCH	CRITICAL	
820-3437	1	PCBF,MLB,J43	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 9 20:06:04 2013

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

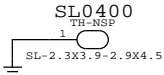
DRAWING TITLE			
<p align="center"><PART_DESCRIPTION></p>			
	<p align="center">Apple Inc.</p>	DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:			
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		BRANCH	<BRANCH>
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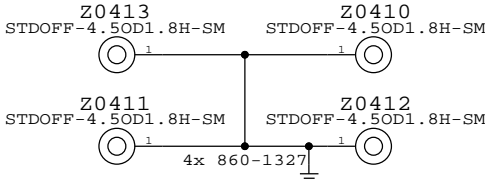
PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

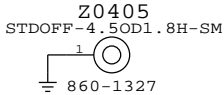
Plated Board Slot



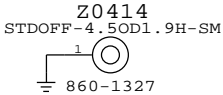
CPU Heat Sink Mounting Bosses



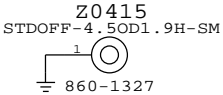
Fan Boss



X21 Boss

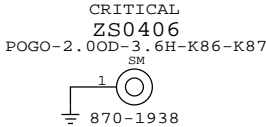
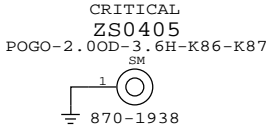


SSD Boss

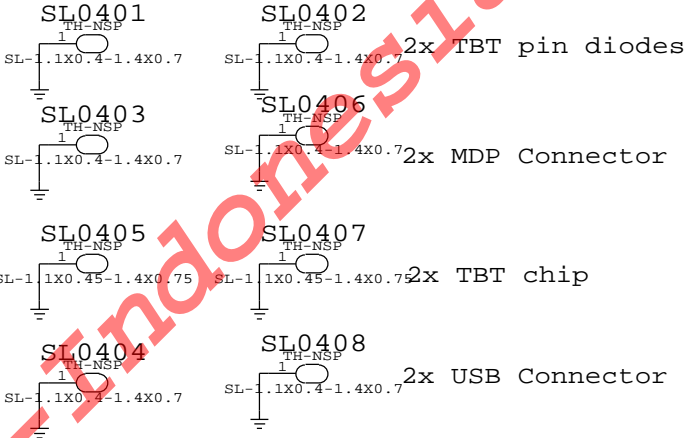


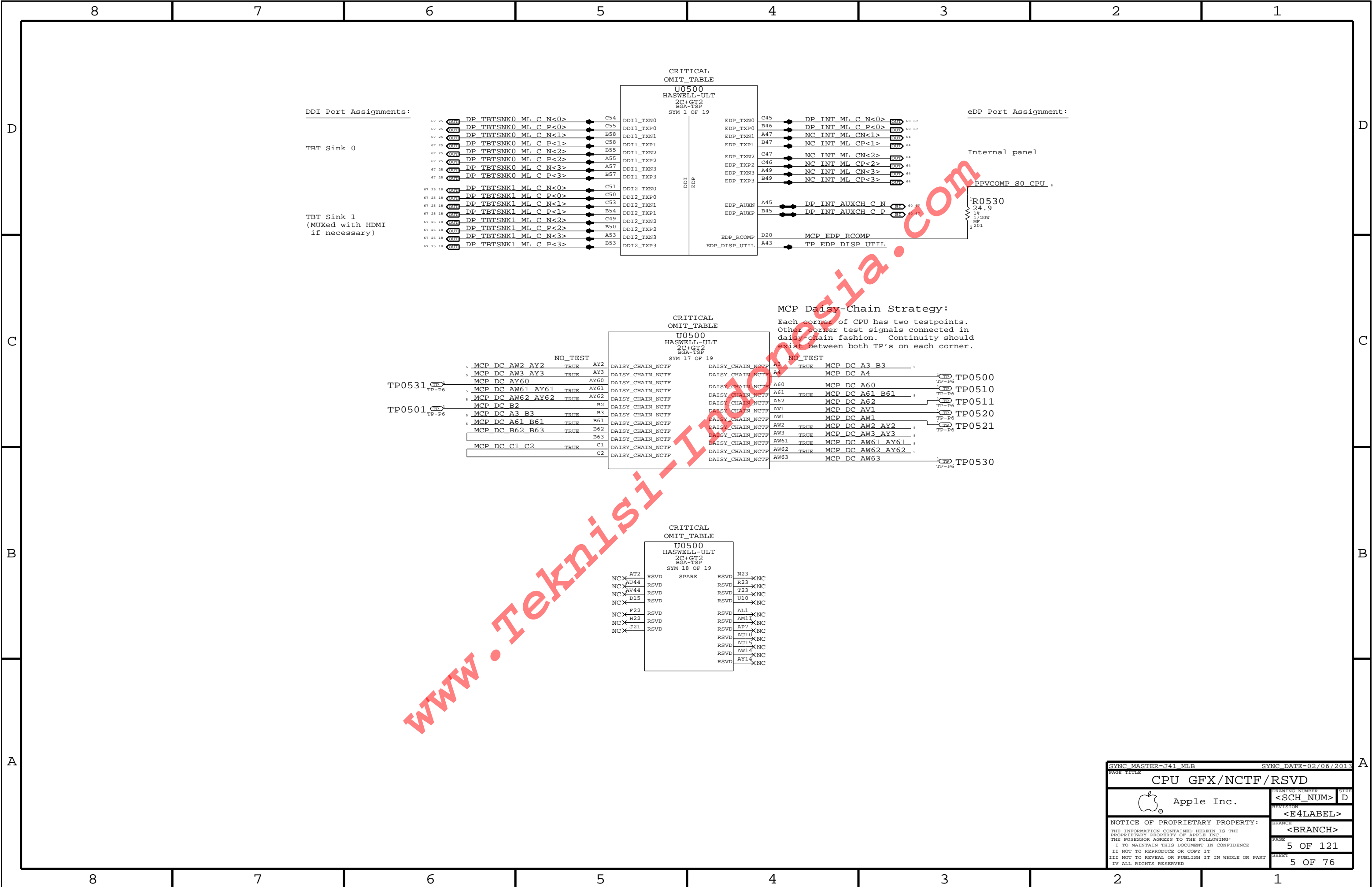
EMI I/O Pogo Pins

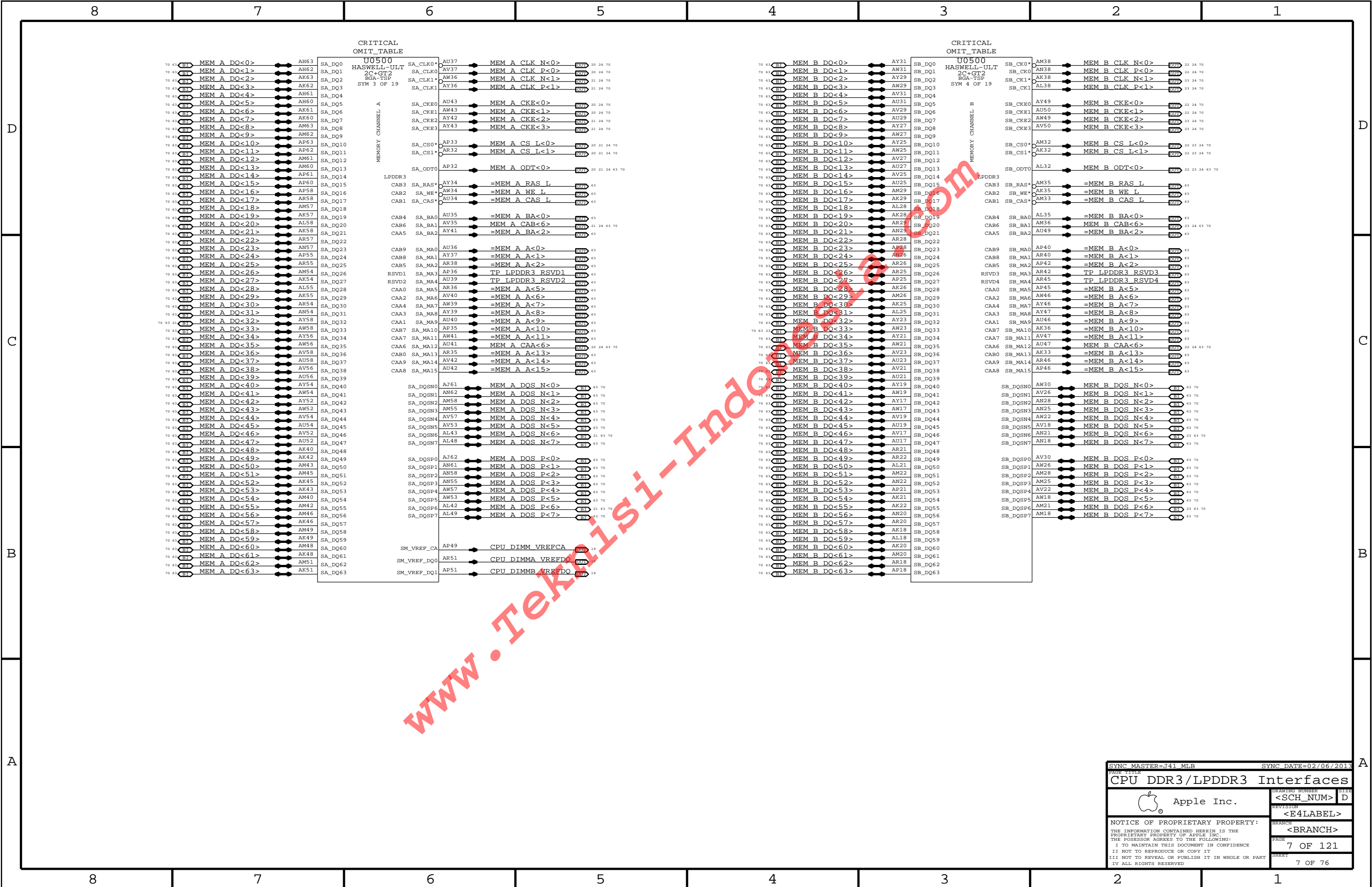
DisplayPort PogoUSB/SD Card Pogo

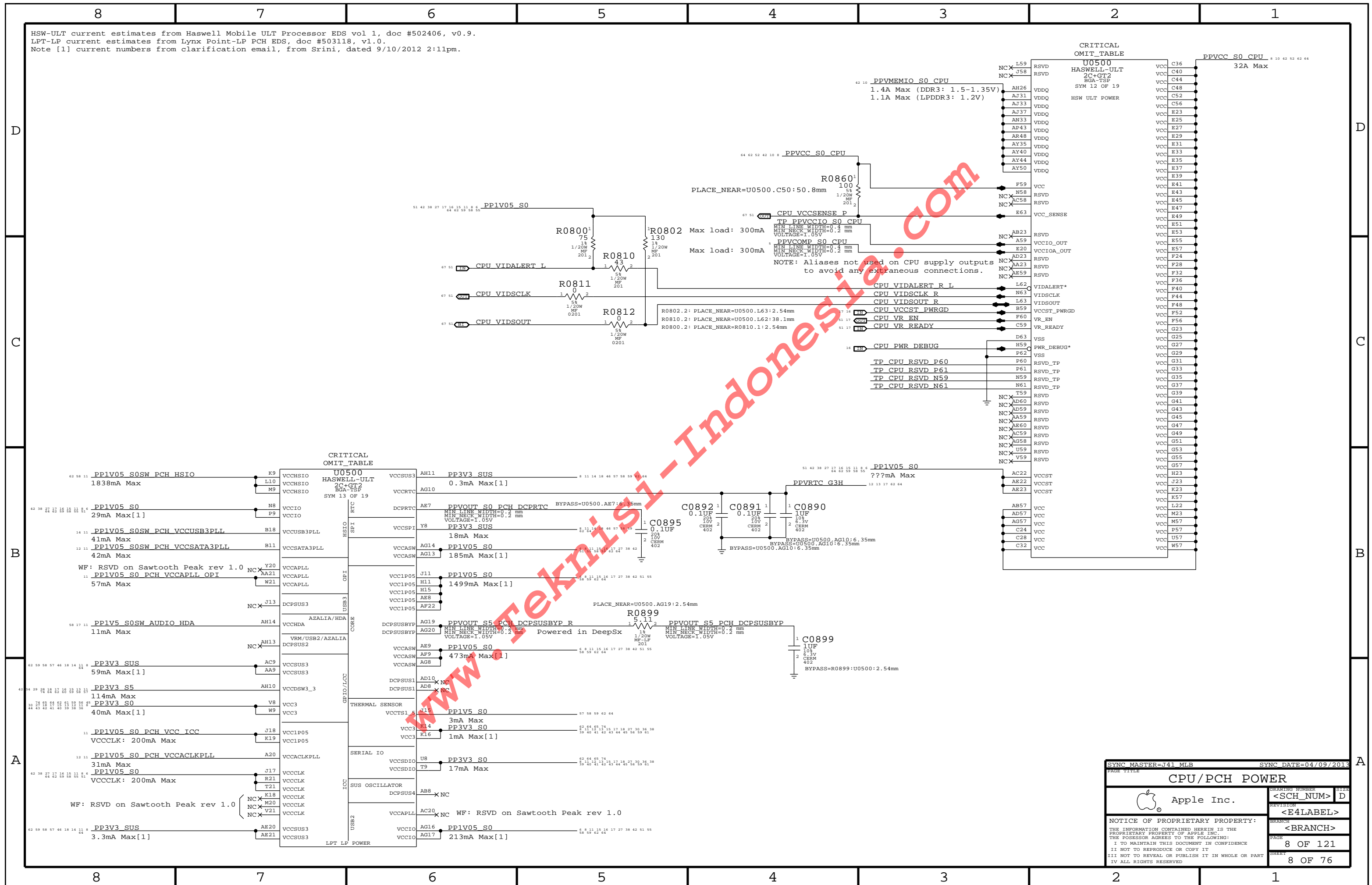


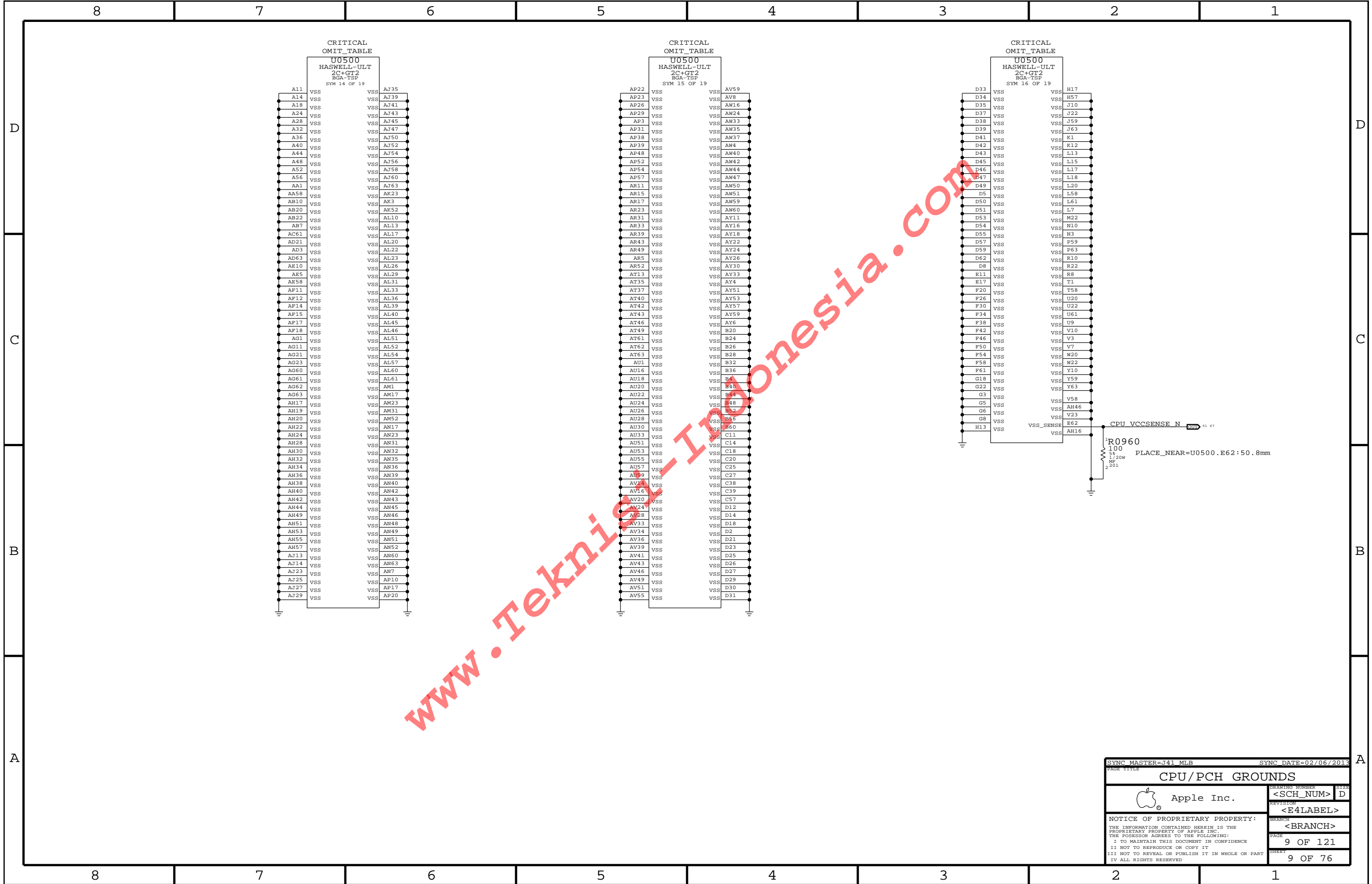
Can Slots

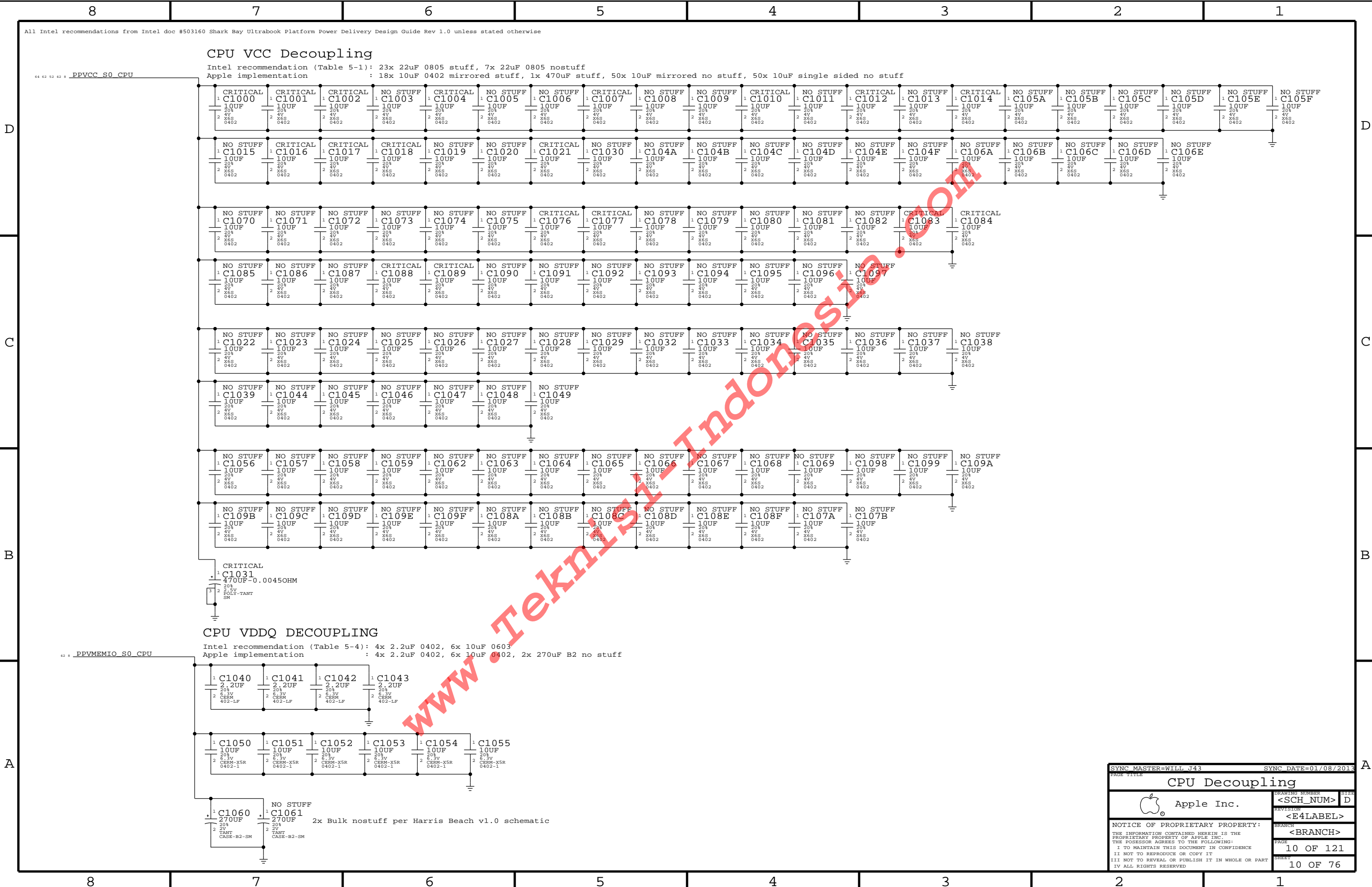





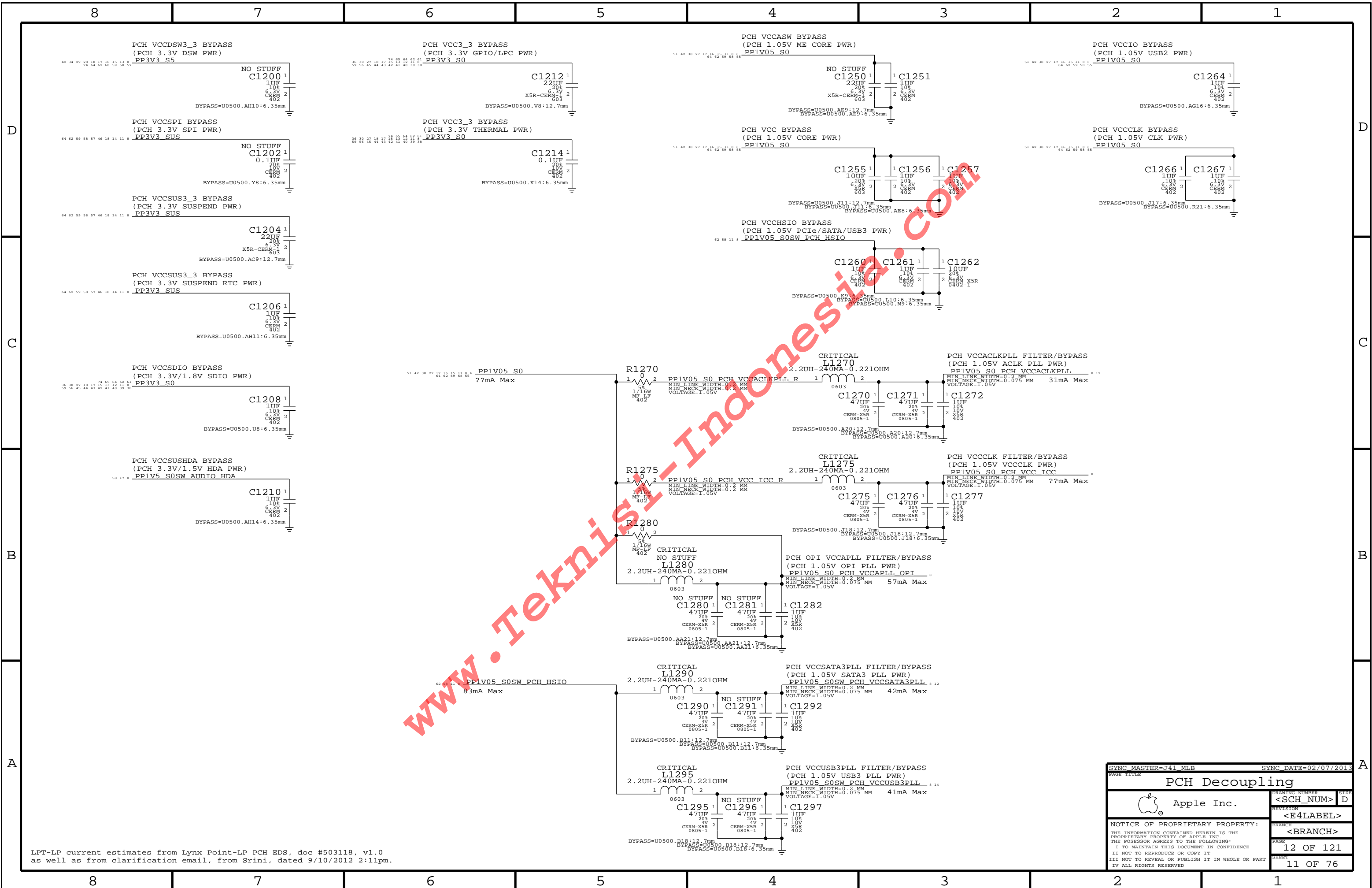







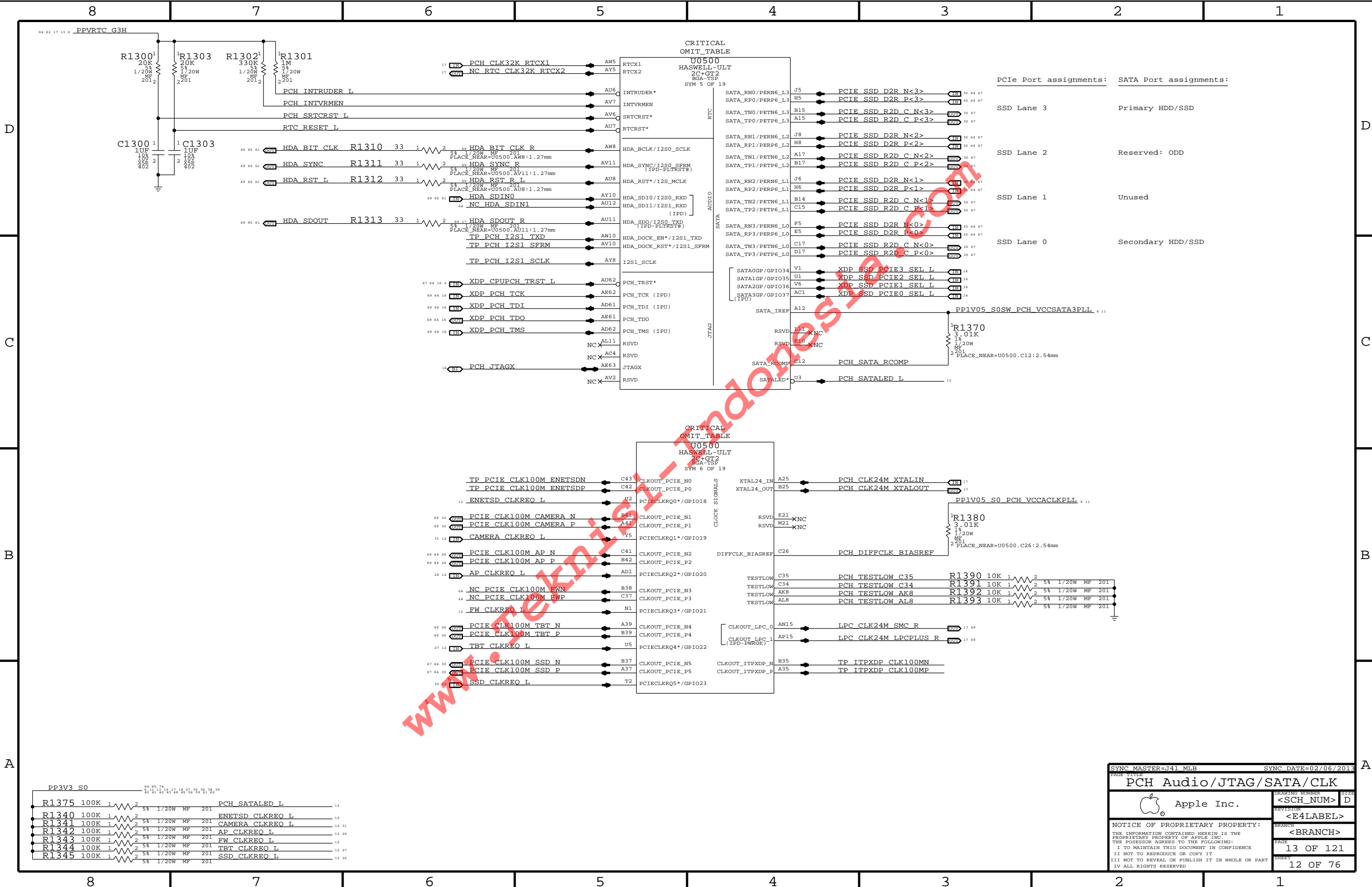



SYNC MASTER=WILL J43		SYNC DATE=01/08/2013			
PAGE TITLE					
CPU Decoupling					
		Apple Inc.			
DRAWING NUMBER		SIZE			
<SCH_NUM>		D			
REVISION		BRANCH			
<E4LABEL>		<BRANCH>			
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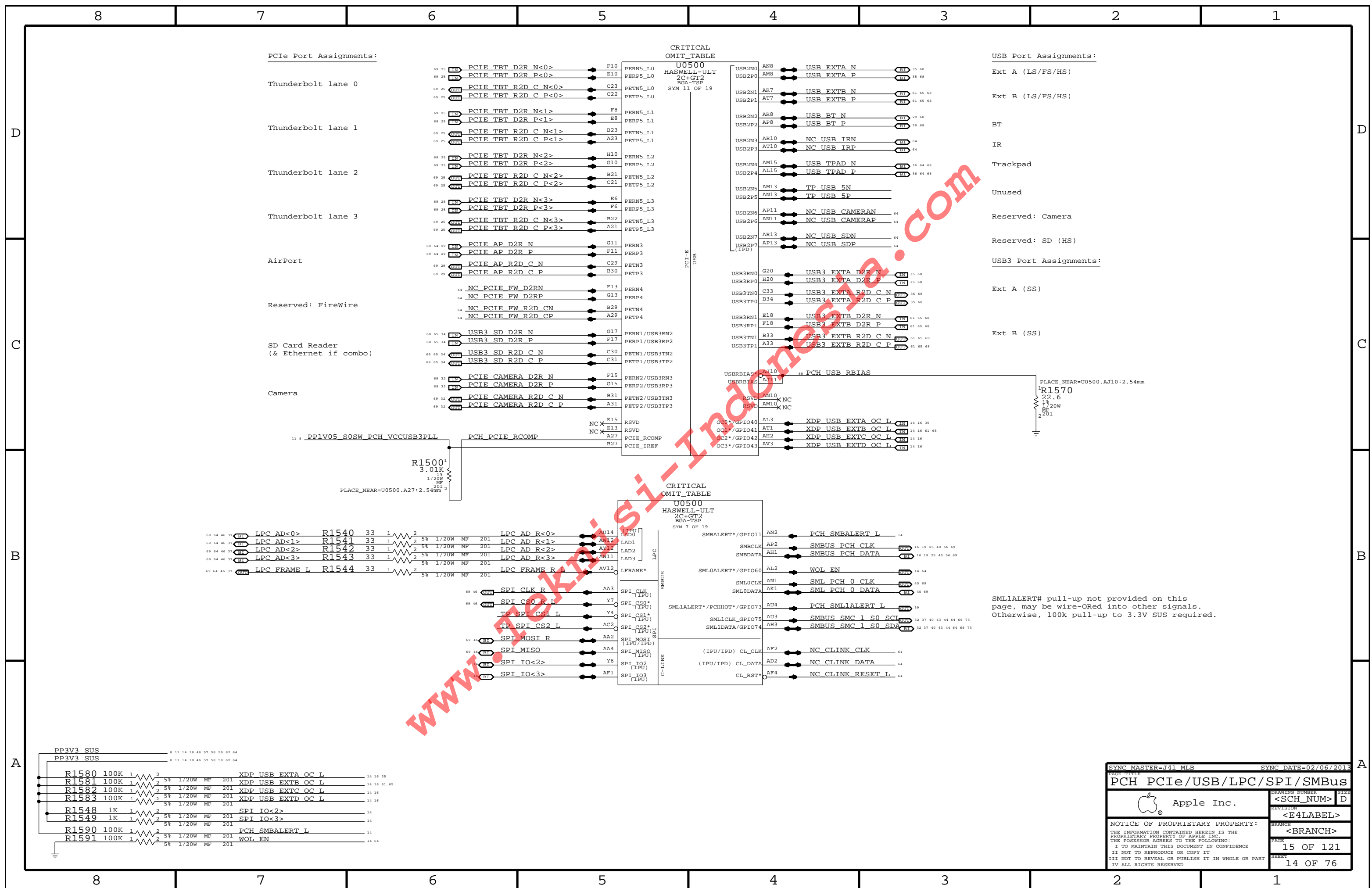


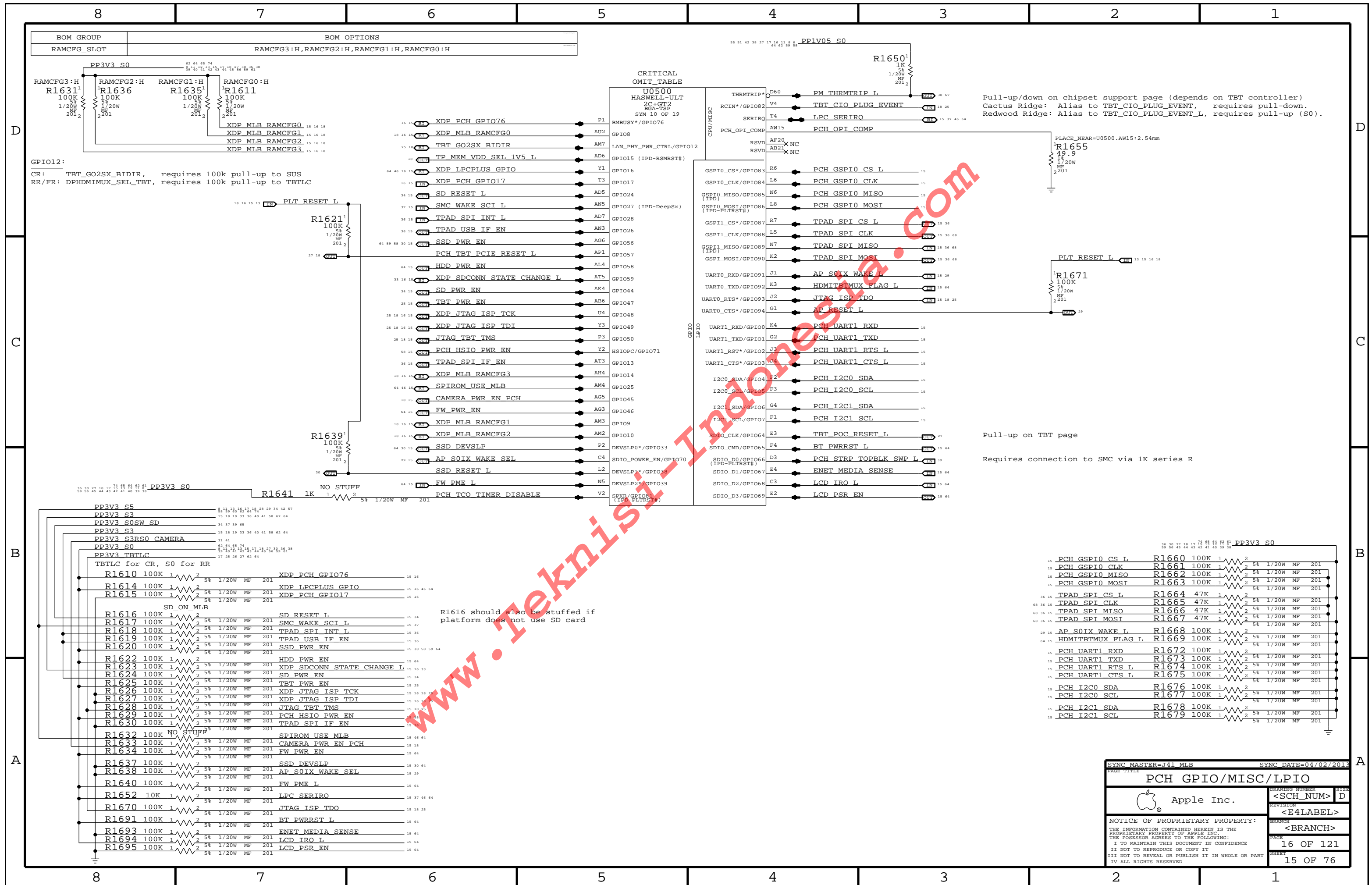
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0 as well as from clarification email, from Srinii, dated 9/10/2012 2:11pm.

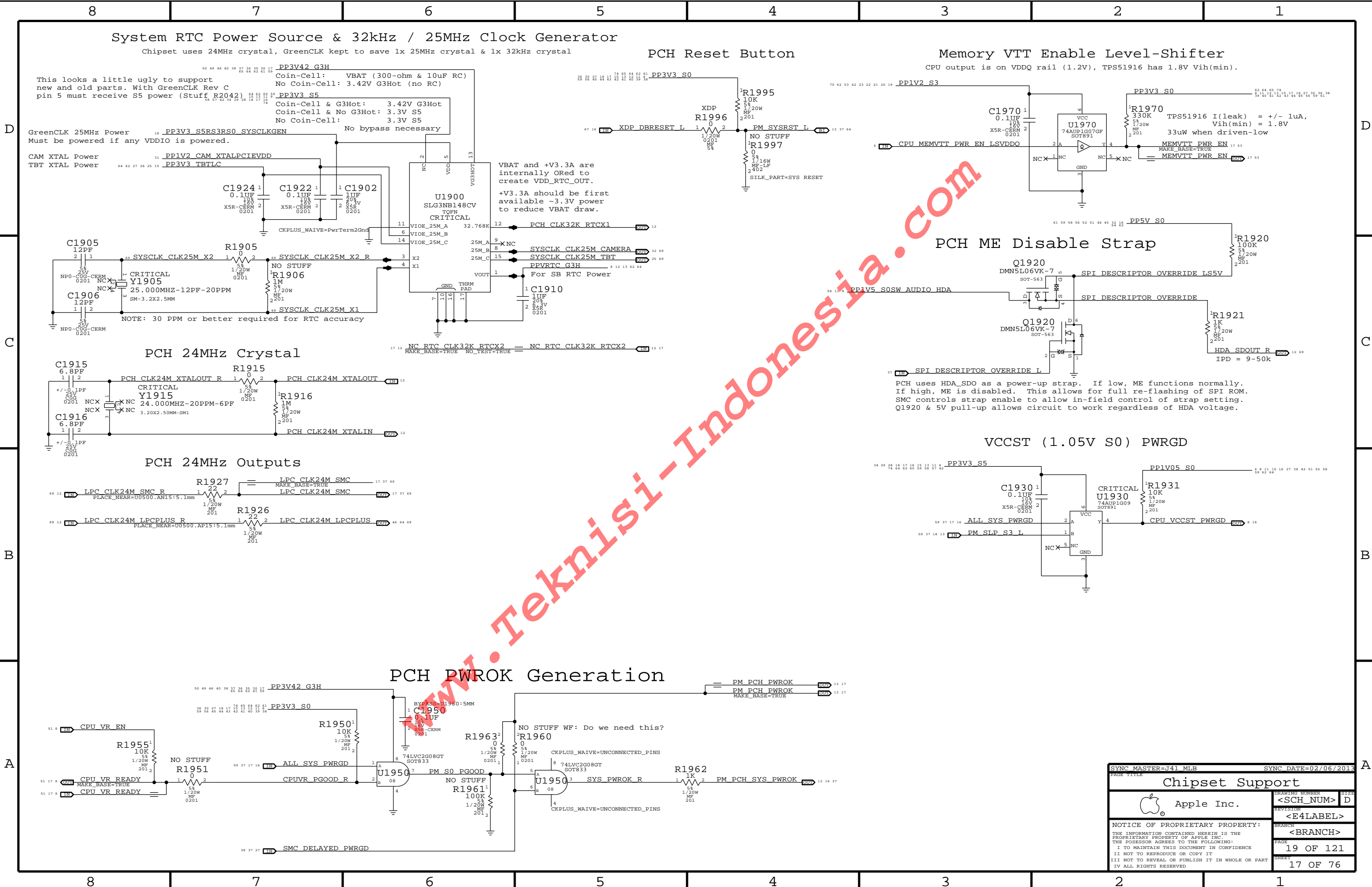
SYNC MASTER=J41 MLB		SYNC DATE=02/07/2013	
PAGE TITLE		PCH Decoupling	
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		<E4LABEL>	<BRANCH>
		PAGE	12 OF 121
		SHEET	11 OF 76

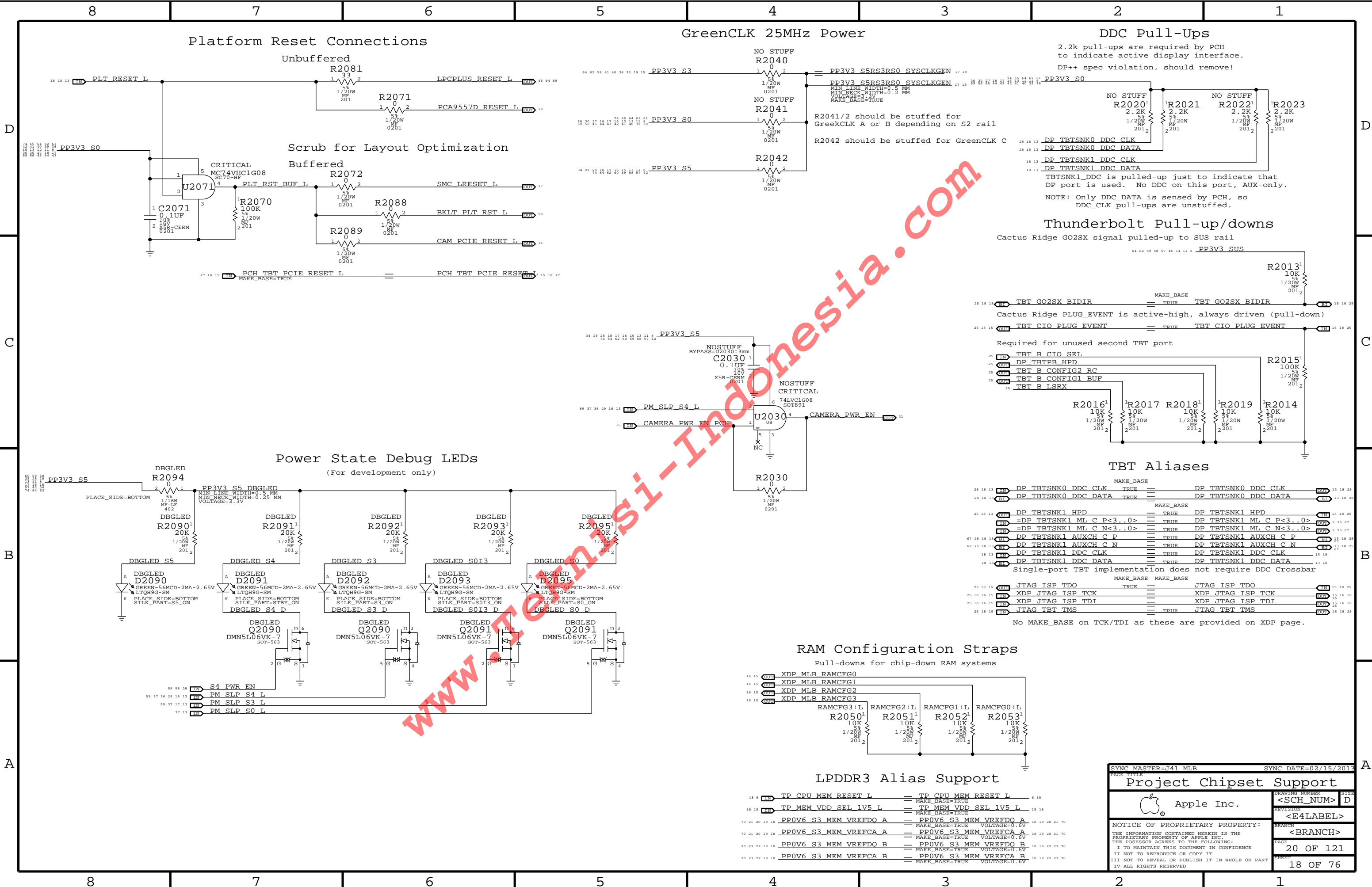


SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
PCH Audio/JTAG/SATA/CLK			
		DRAWING NUMBER	
Apple Inc.		<SCH_NUM>	
		REVISION	
		<E4LABEL>	
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		<BRANCH>	
		PAGE	
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Power aliases required by this page:

- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:

- =I2C_VREFDAC_S_SCL
- =I2C_VREFDAC_S_SDA
- =I2C_PCA9557D_S_SCL
- =I2C_PCA9557D_S_SDA

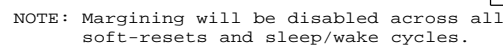
BOM options provided by this page:

- DDRVREF_DAC - Stuffs DAC margining circuit.

FETs for CPU isolation during DAC margining

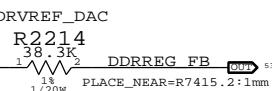
NOTE: CPU has single output for VREFOCA. Split into two signals for independent DAC margining support. When DAC margining VREFOCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.


DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



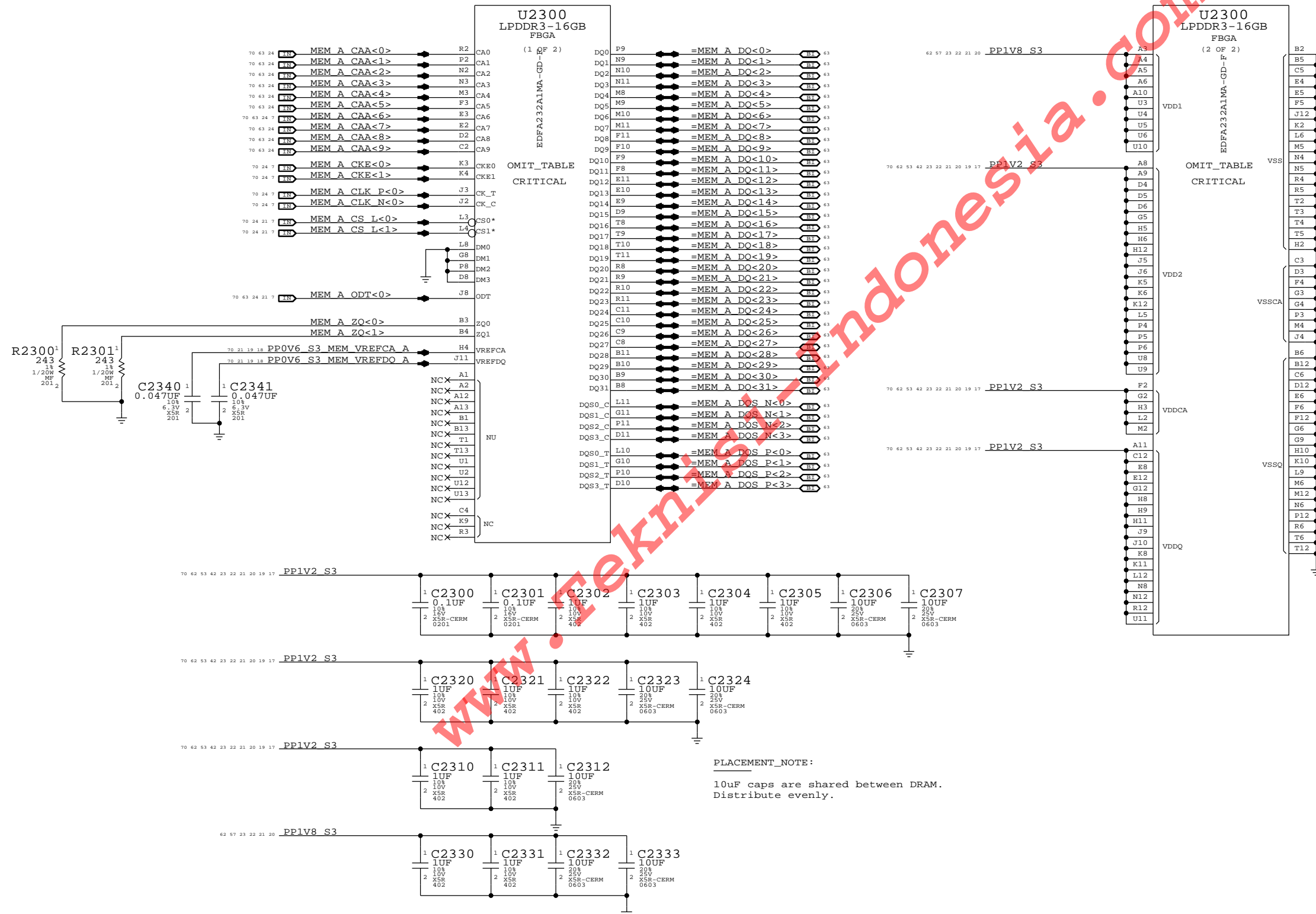
NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider


Always used, regardless
of margining option.



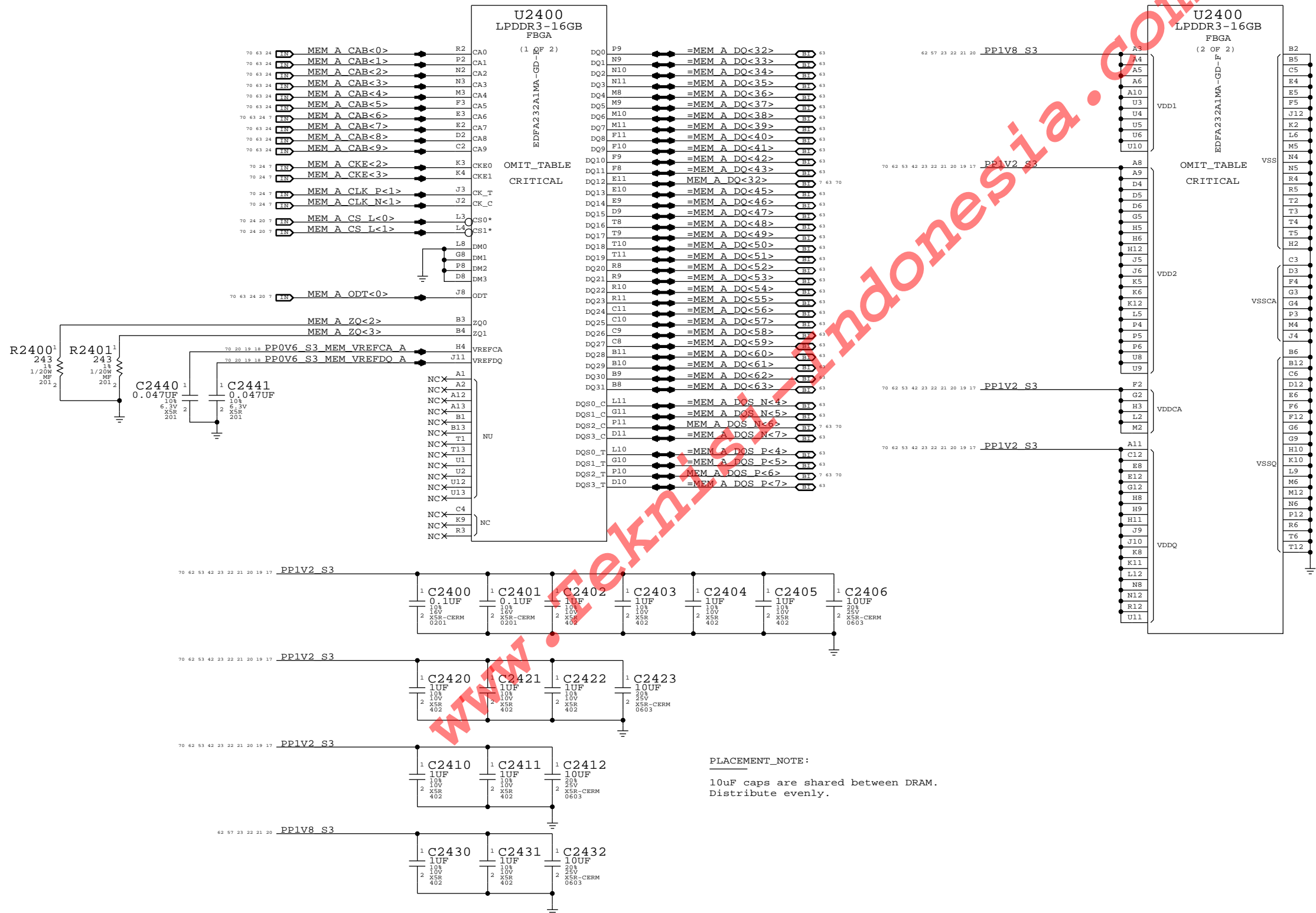
SYNC_MASTER=J41 MLB		SYNC_DATE=02/12/2013	
PAGE TITLE			
DDR3 VREF MARGINING			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		SIZE D	
		REVISION <E4LABEL>	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
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LPDDR3 CHANNEL A (0-31)

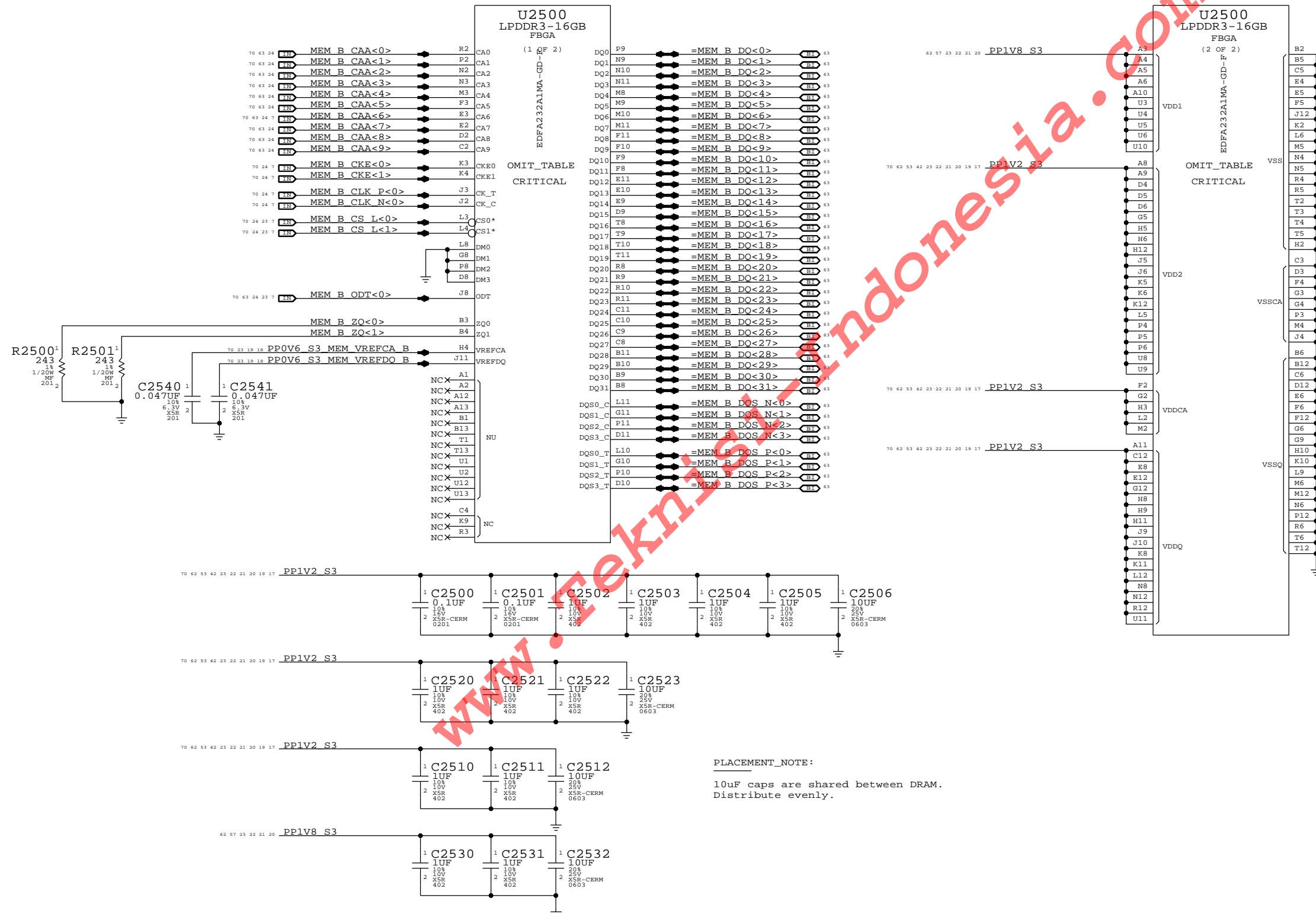


SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
LPDDR3 DRAM Channel A (0-31)			
 Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
	REVISION	<E4LABEL>	
	BRANCH	<BRANCH>	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE	23 OF 121
		SHEET	20 OF 76

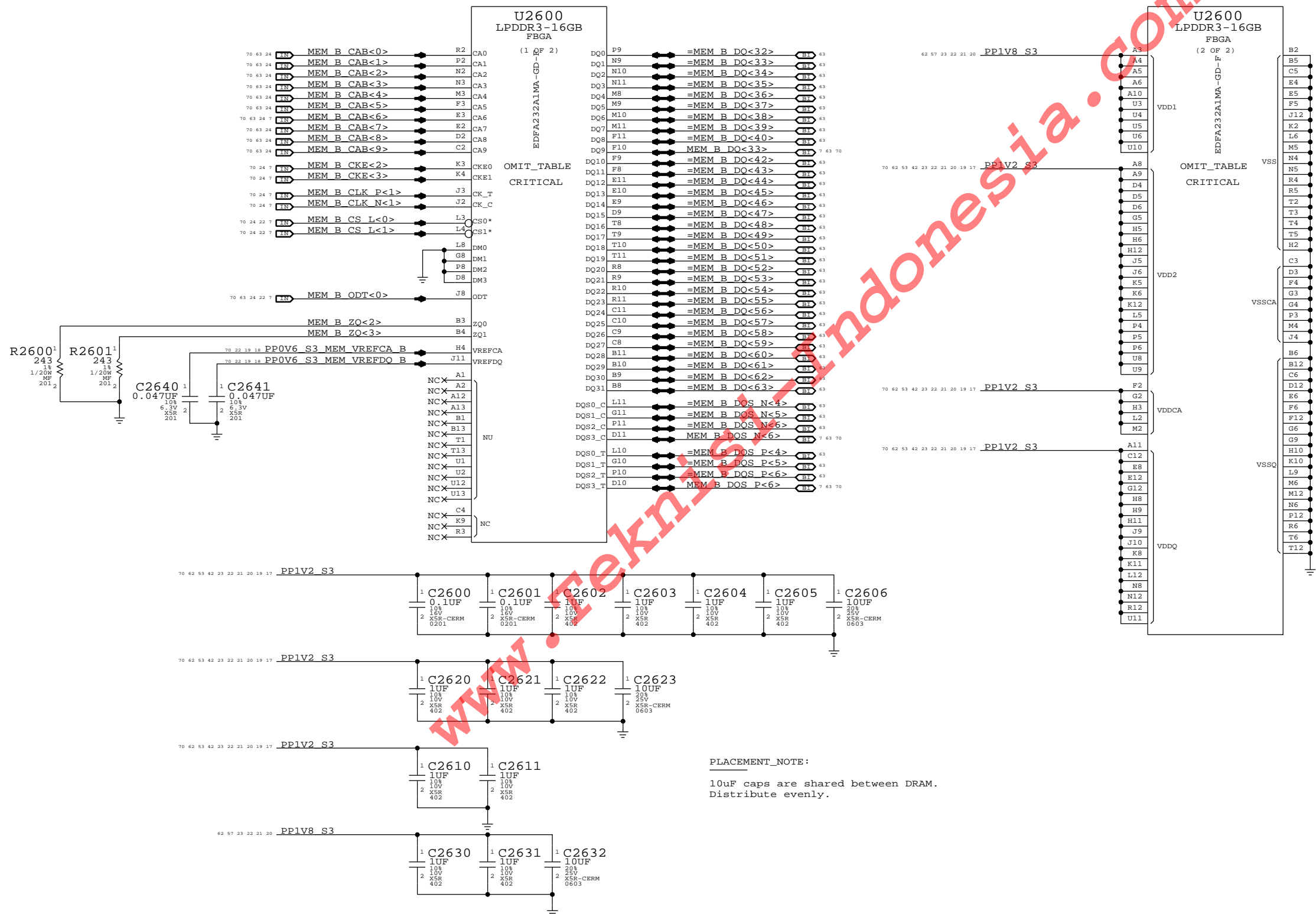
LPDDR3 CHANNEL A (32-63)

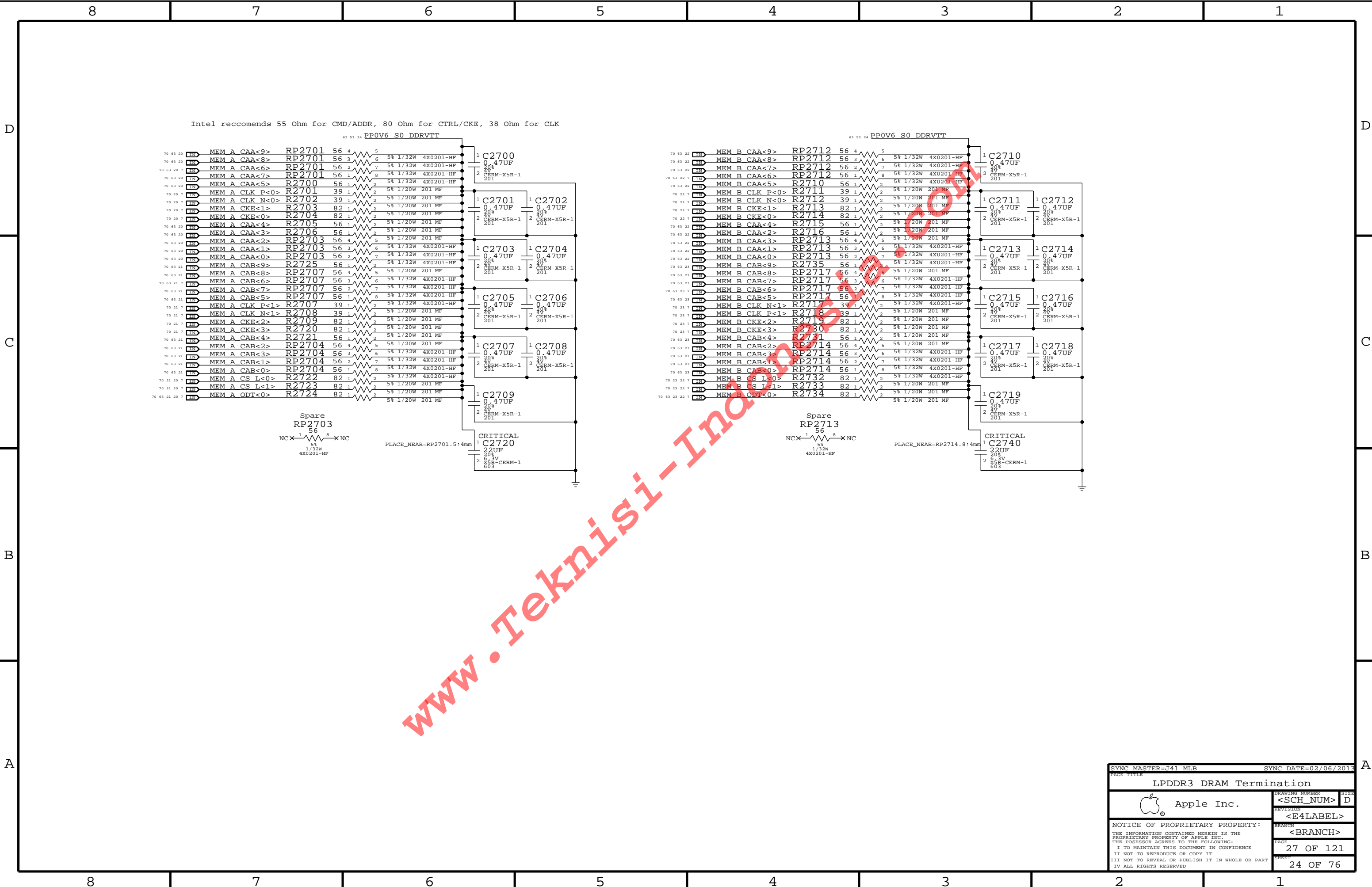


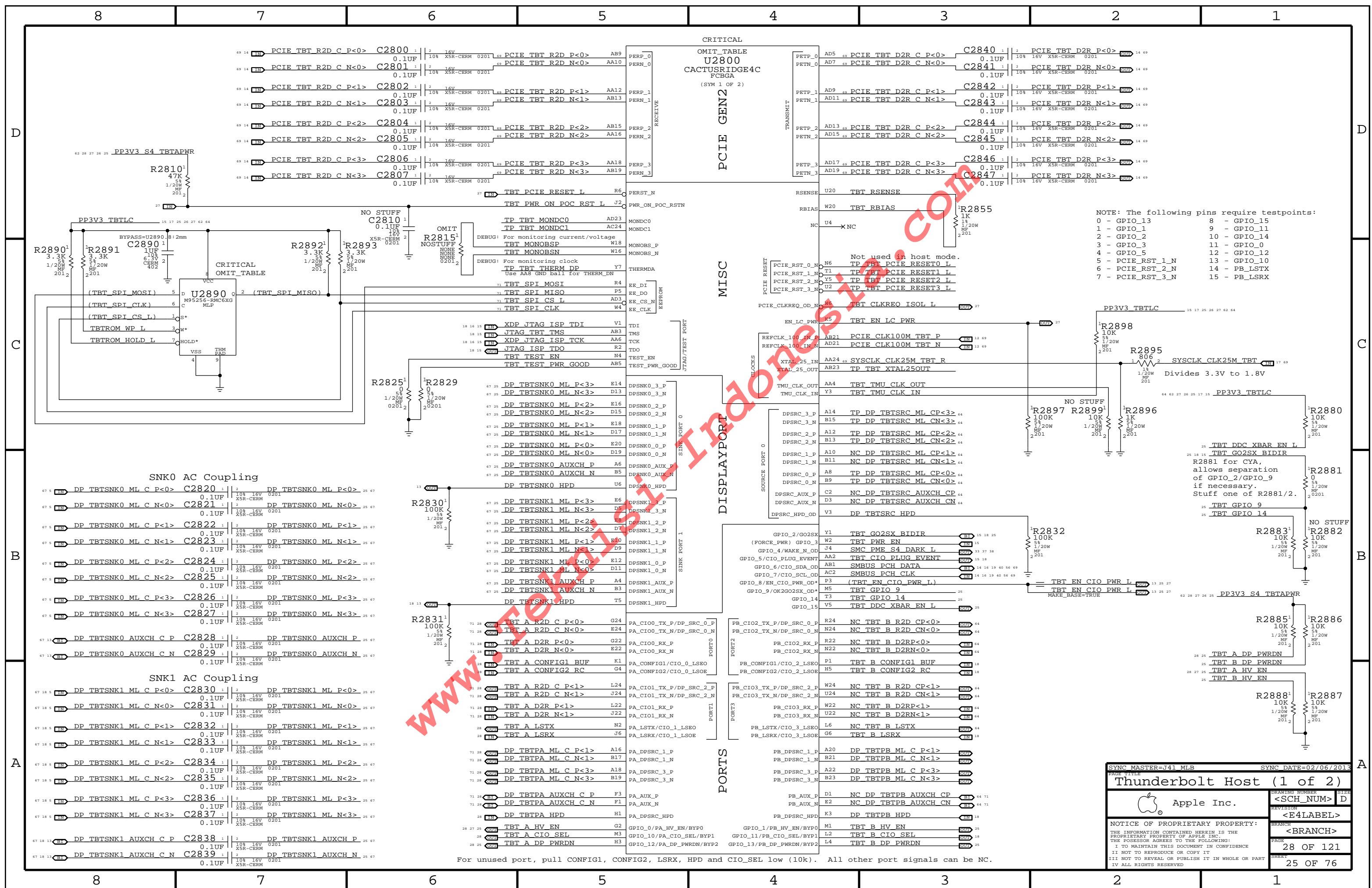
LPDDR3 CHANNEL B (0-31)

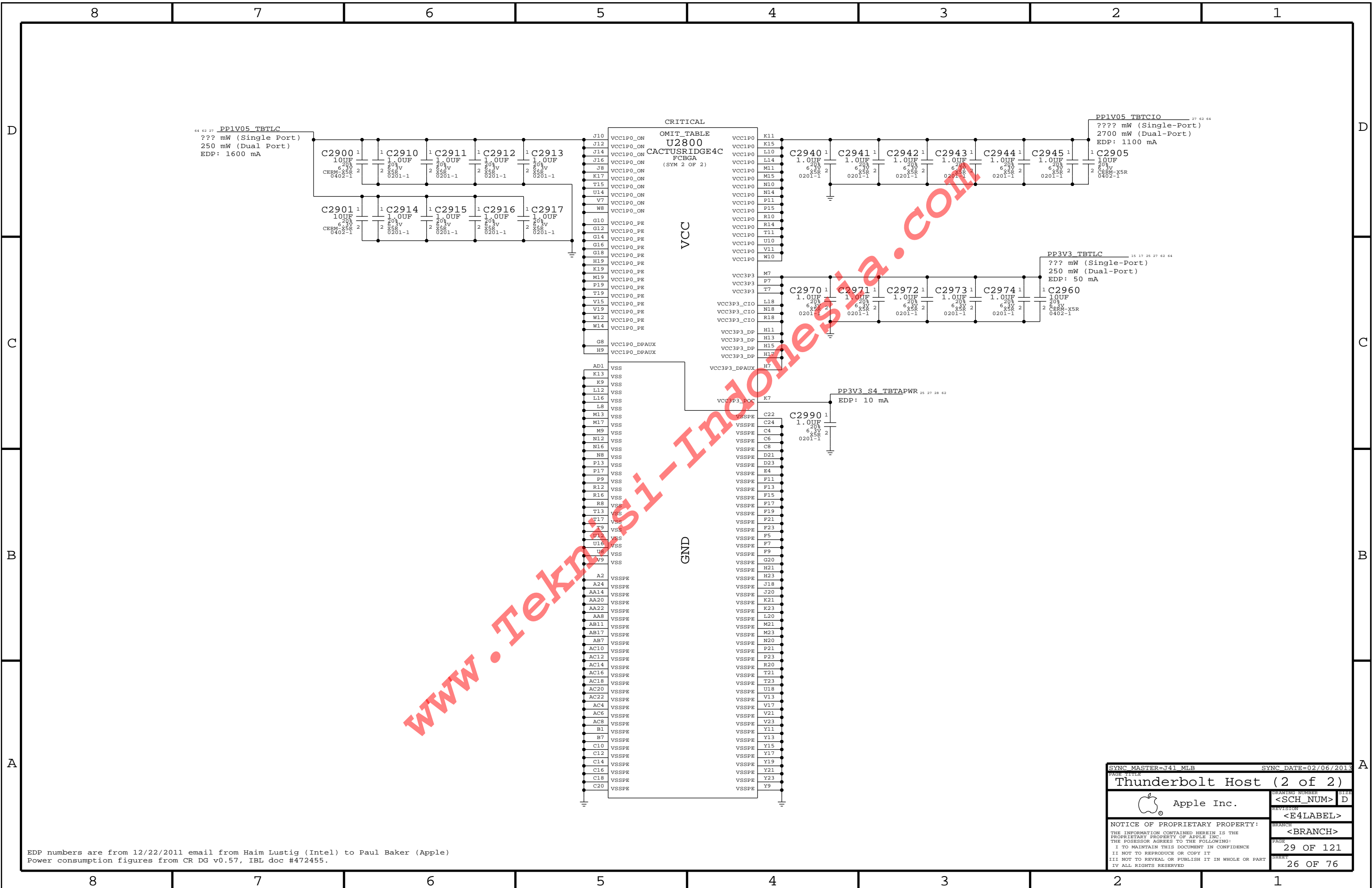


LPDDR3 CHANNEL B (32-63)










EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=J41 MLB

SYNC DATE=02/06/2013

Thunderbolt Host (2 of 2)

 Apple Inc.

DRAWING NUMBER<SCH_NUM>

REVISION<E4LABEL>

BRANCH<BRANCH>

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTTPWRCTL (3.3V FET Input)
- =PP1V05_TBT_P1V05TBTFTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

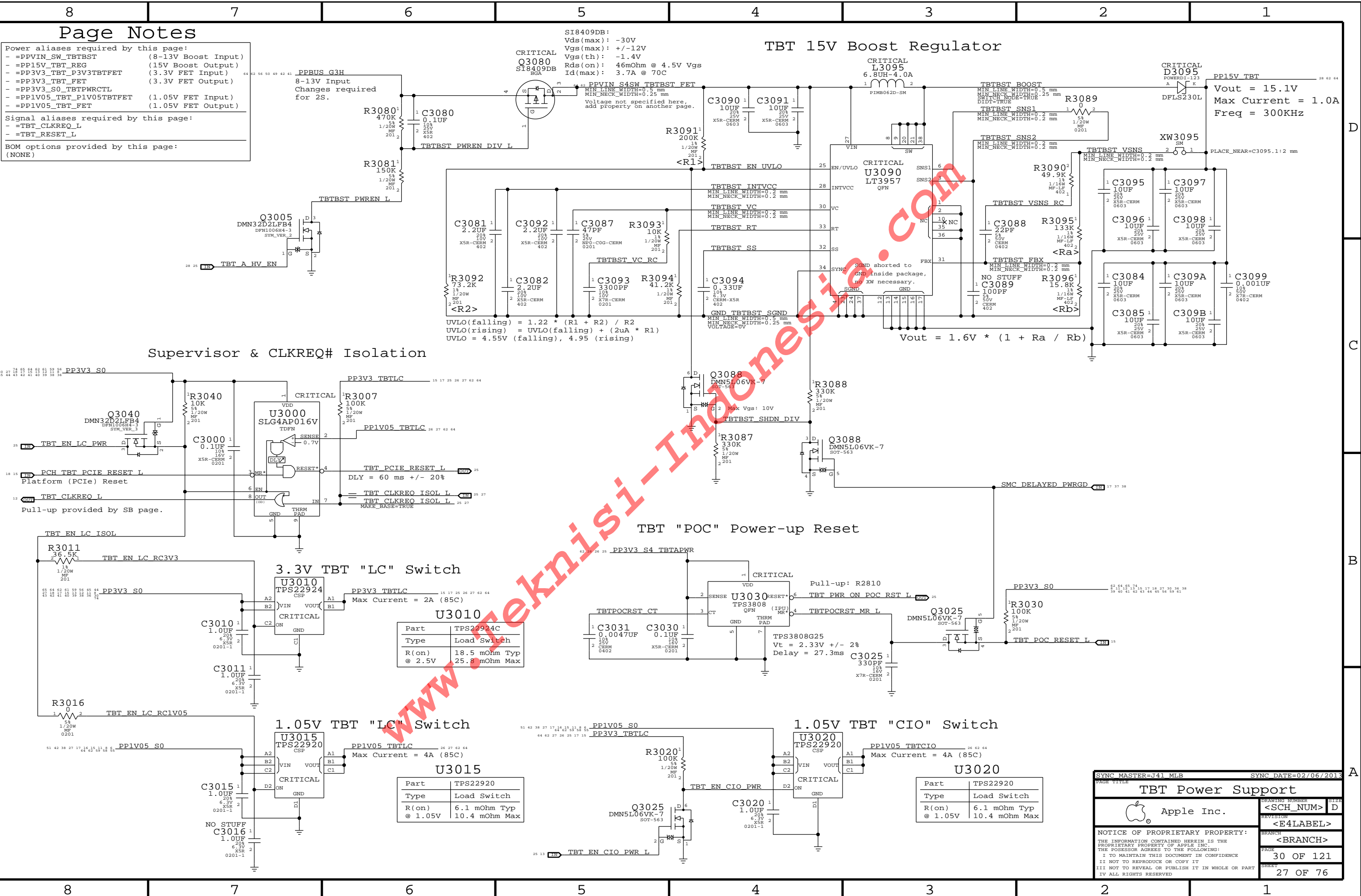
BOM options provided by this page:
(NONE)

D

C

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D

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A

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
TBT Power Support			
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	30 OF 121
		SHEET	27 OF 76
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D



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

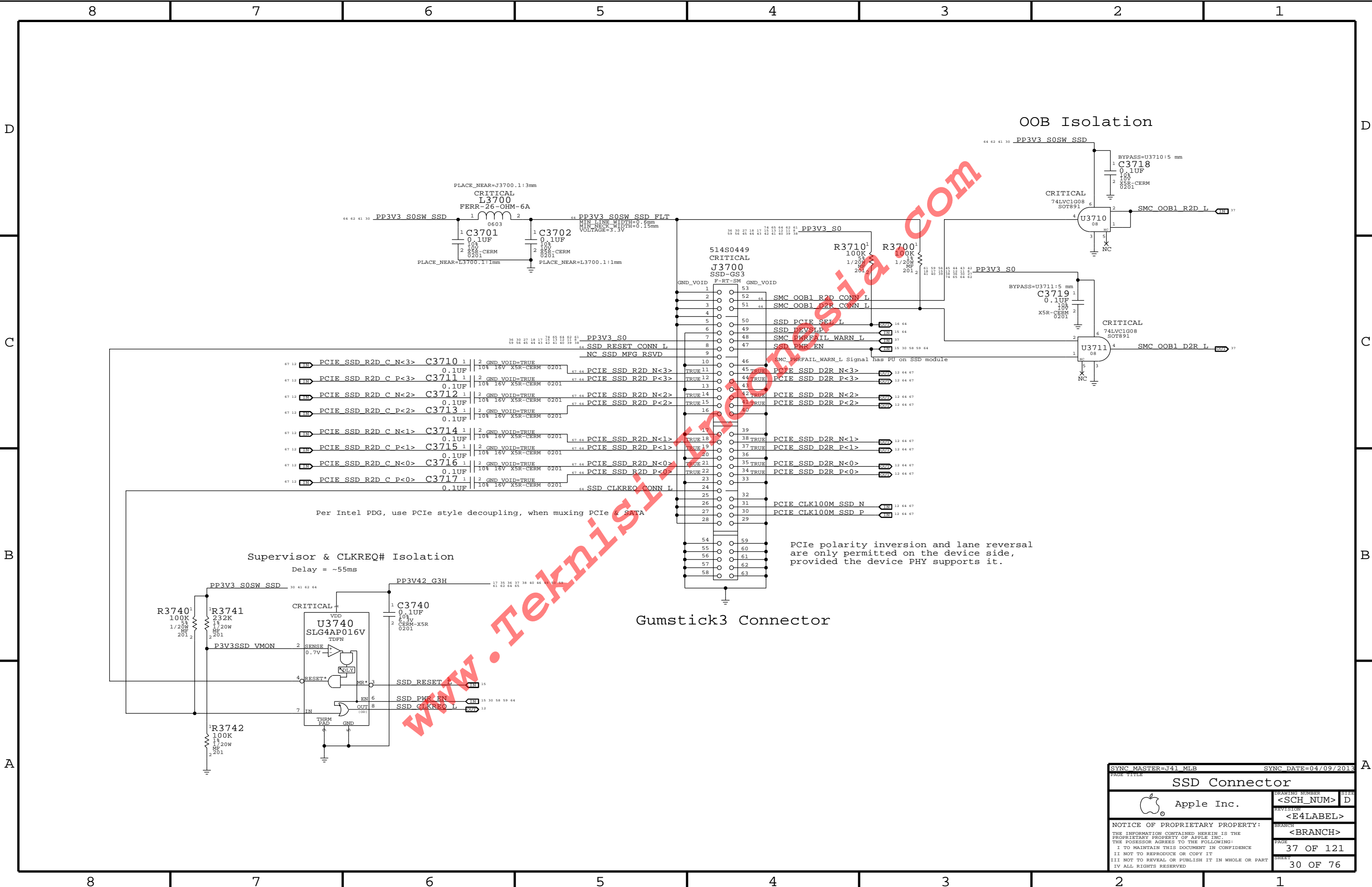



C

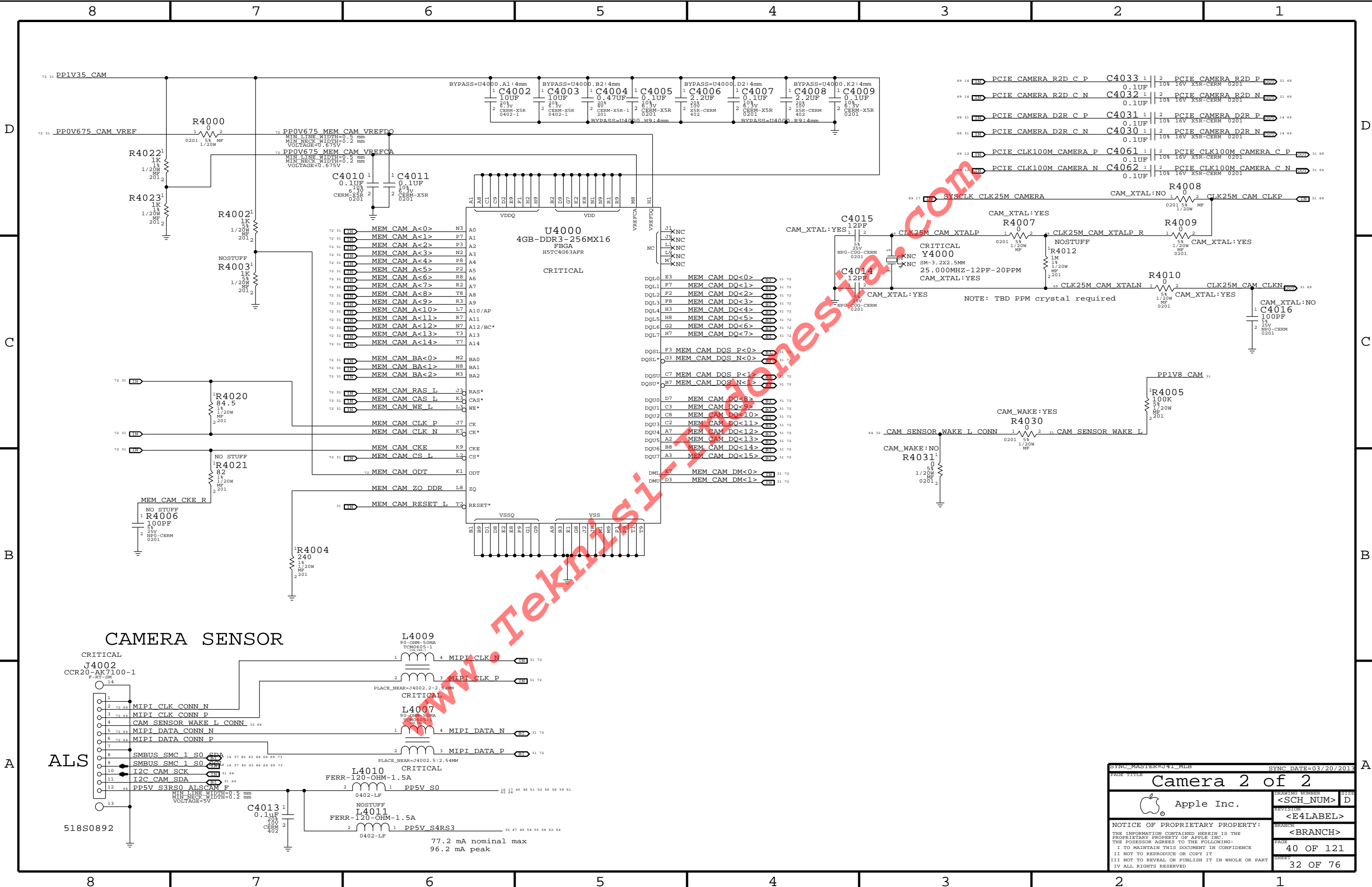


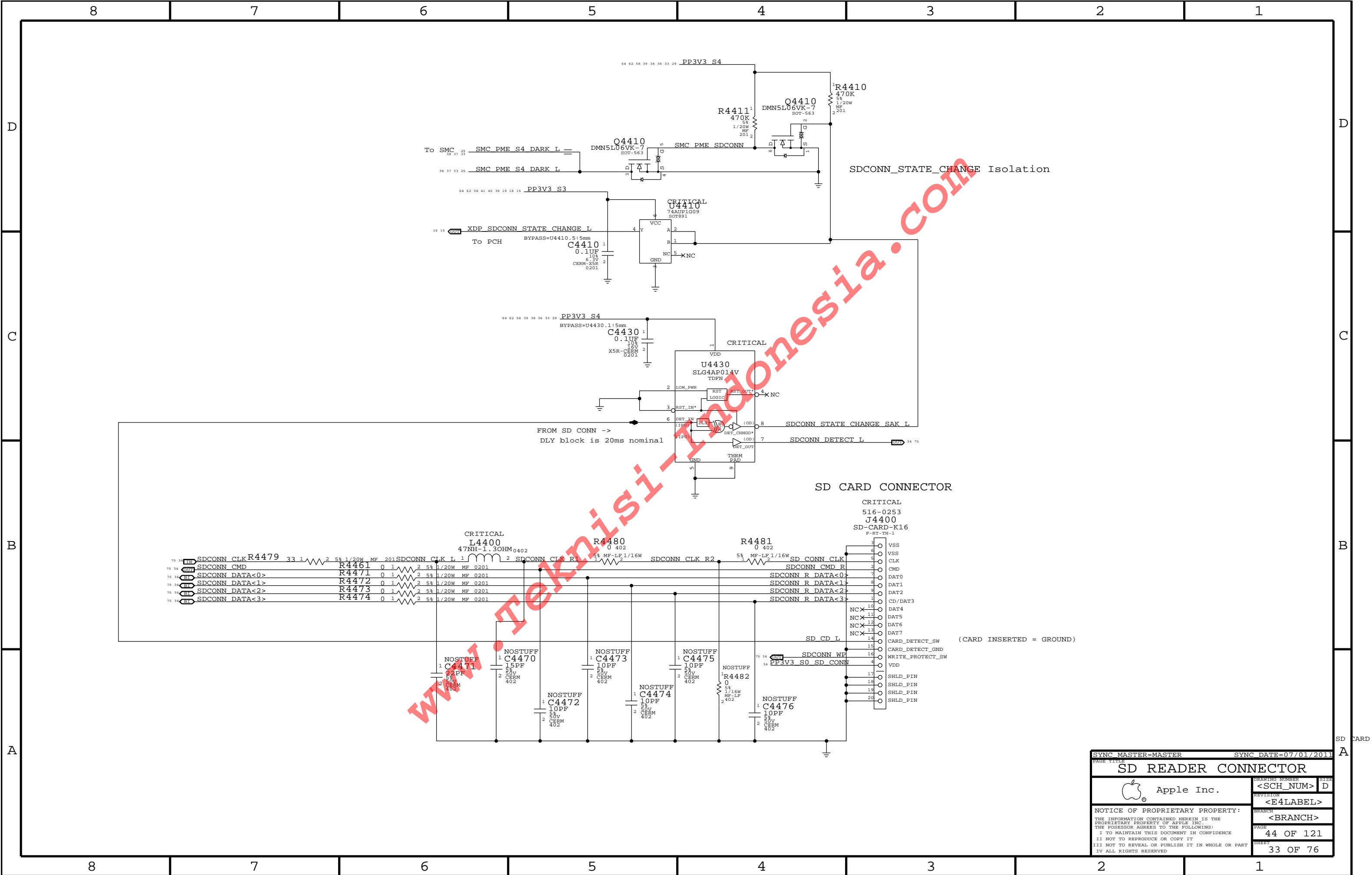
A


A



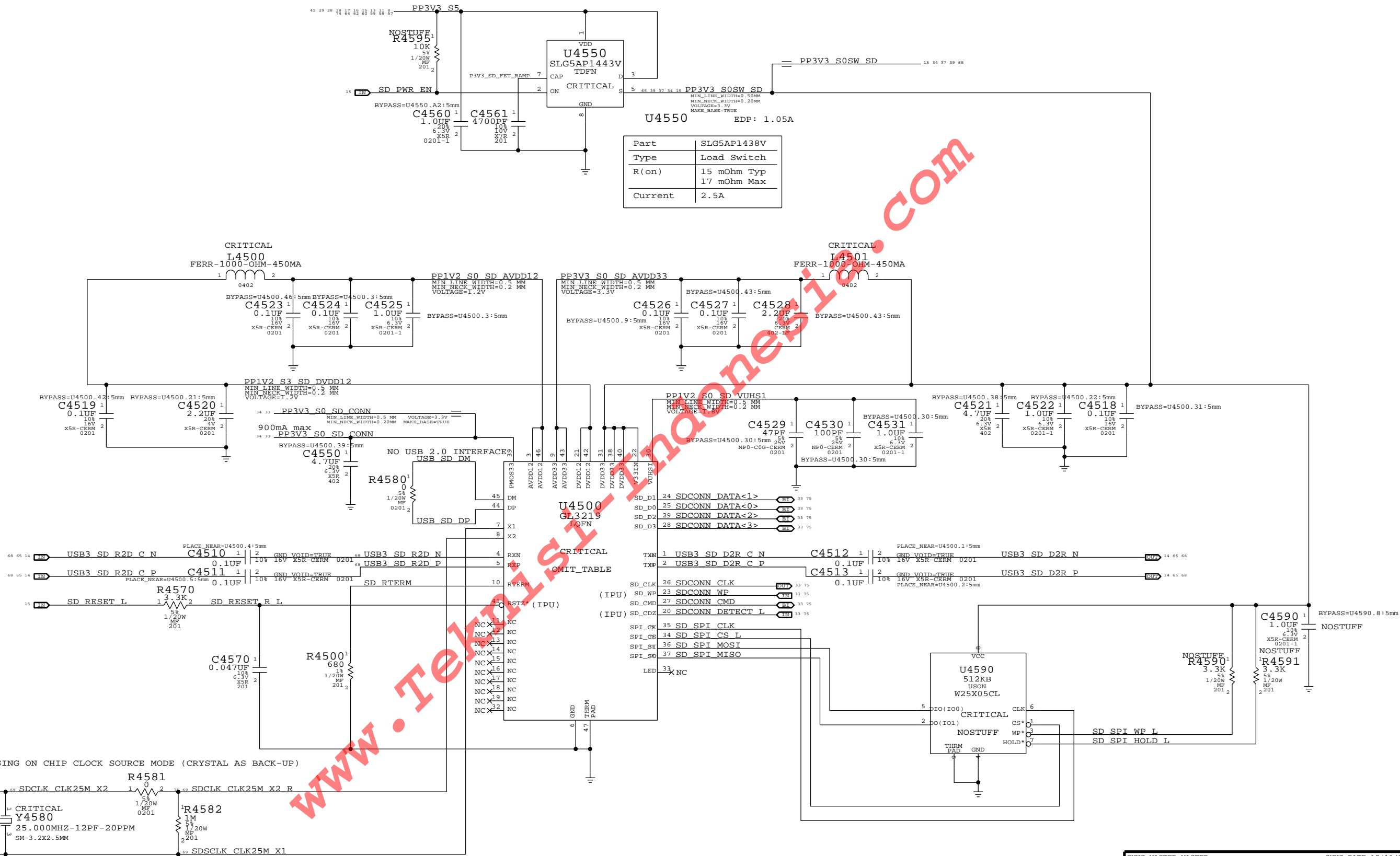
SYNC MASTER=J41 MLB		SYNC DATE=04/09/2013	
PAGE TITLE			
SSD Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		<E4LABEL>	
		BRANCH	
		<BRANCH>	
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SYNC MASTER=MASTER		SYNC DATE=07/01/2011	
PAGE TITLE			
SD READER CONNECTOR			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	44 OF 121
		SHEET	33 OF 76

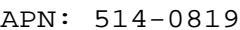
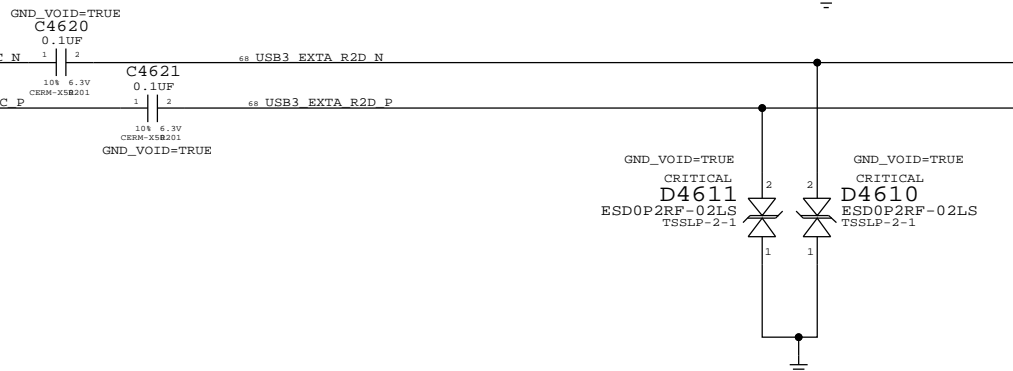
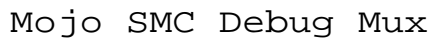
3.3V S3 SD Card Switch

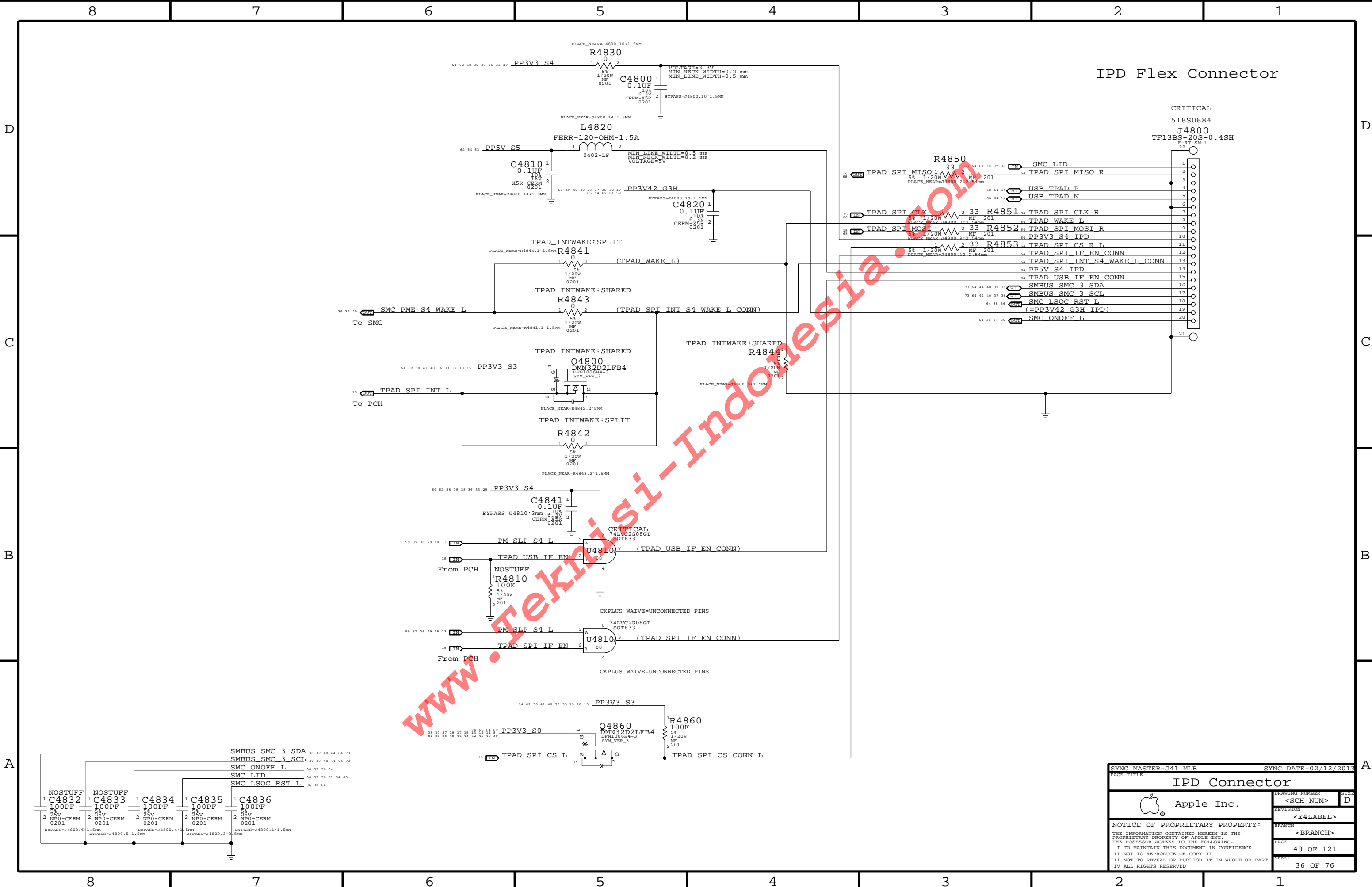


Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ
Current	2.5A

SYNC MASTER=MASTER		SYNC DATE=10/11/2010	
PAGE TITLE			
SD CONTROLLER		(GL3219)	
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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		PAGE	45 OF 121
		SHEET	
			34 OF 76


USB Port Power Switch

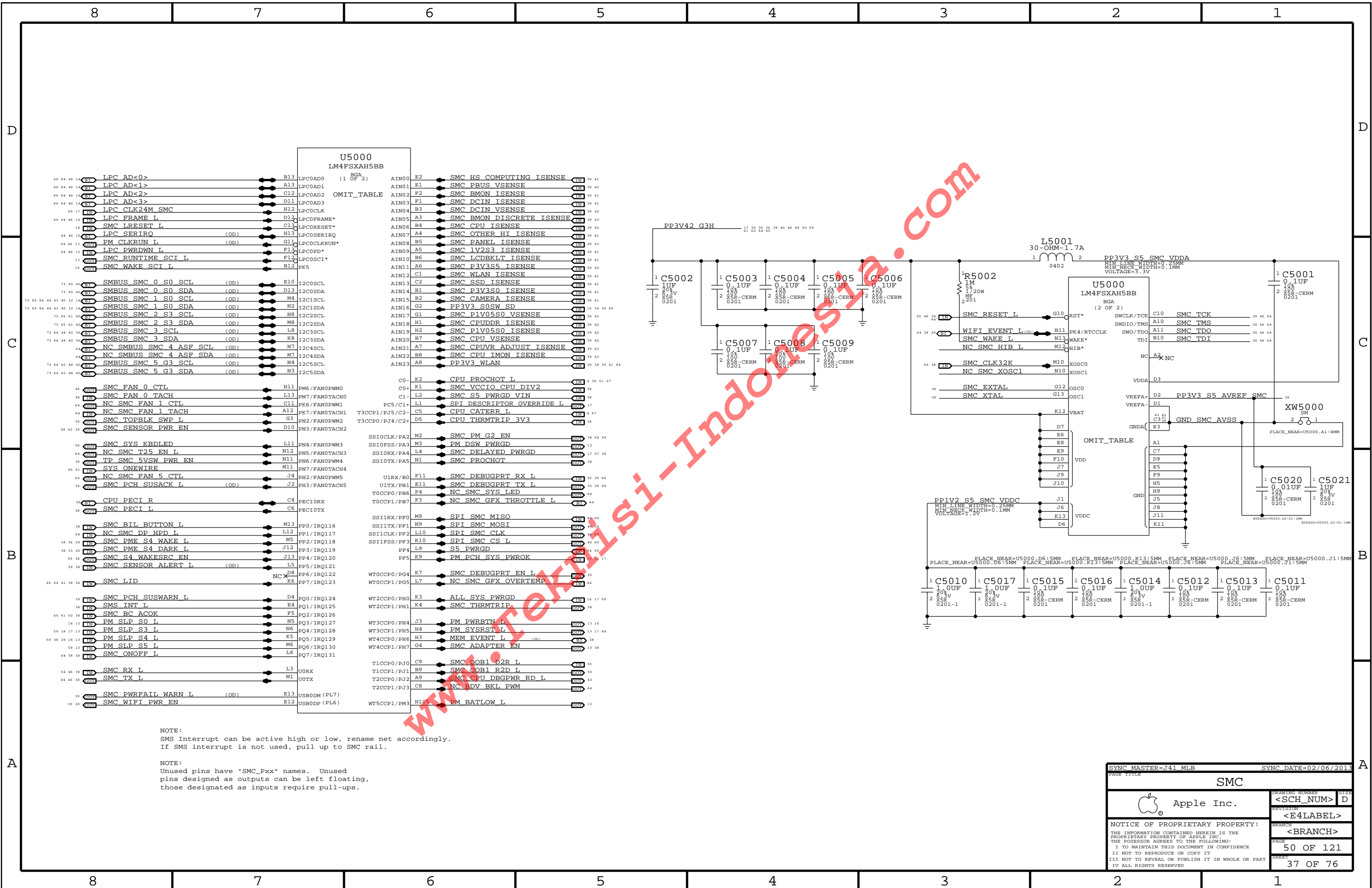


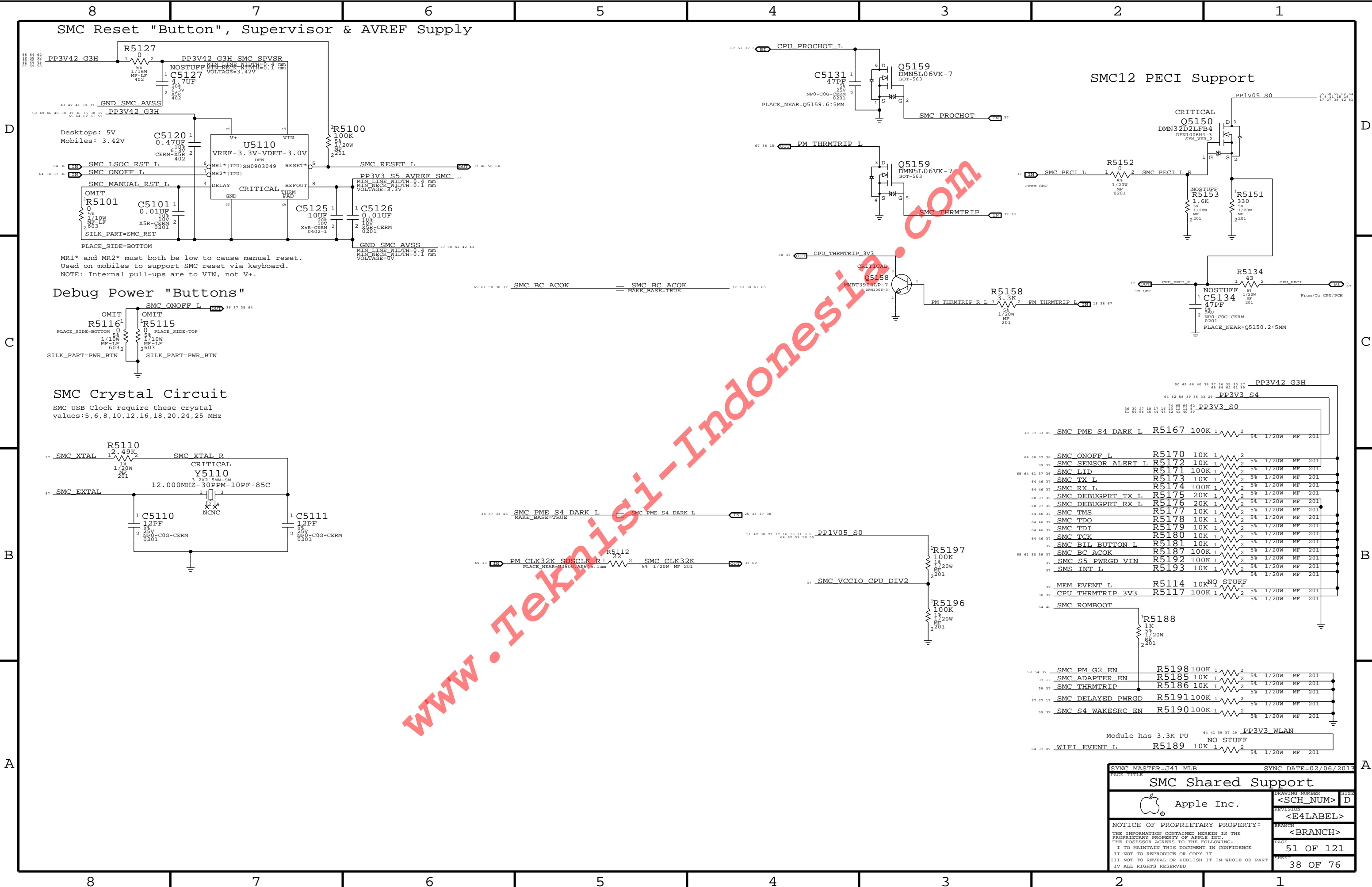


IPD Flex Connector

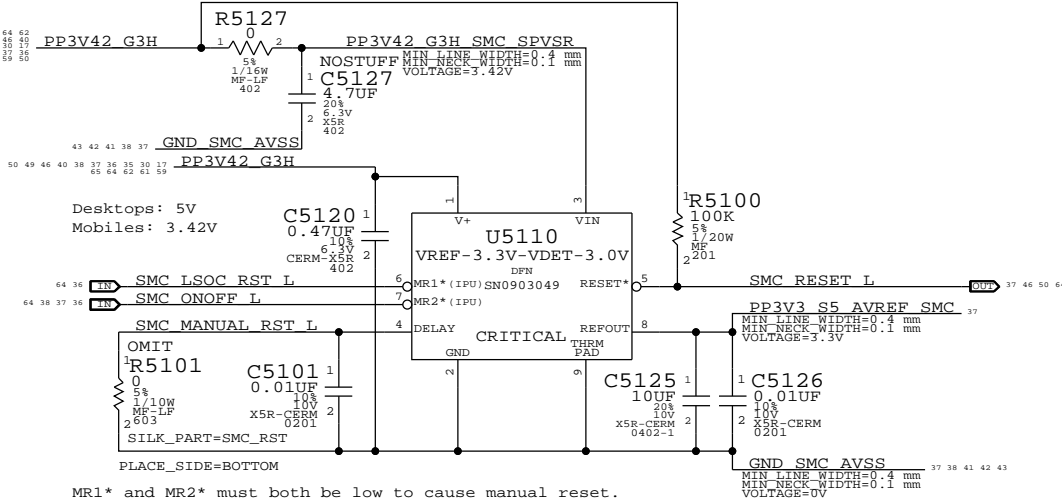
CRITICAL	
518S0884	
J4800	
TF13BS-20S-0.4SH	
F-RT-SM-1	
22	
1	
2	
3	
4	
5	
6	
7	
8	
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SYNC MASTER=J41 MLB		SYNC DATE=02/12/2013	
PAGE TITLE			
IPD Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	48 OF 121
		SHEET	36 OF 76
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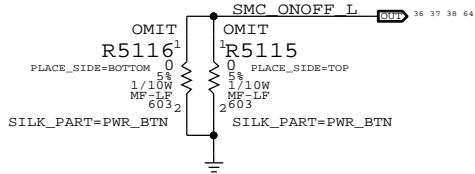




SMC Reset "Button", Supervisor & AVREF Supply

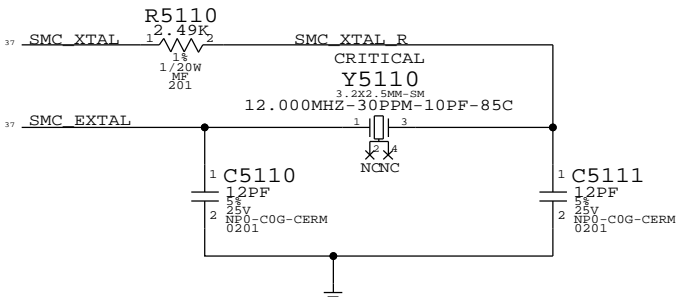


Debug Power "Buttons"

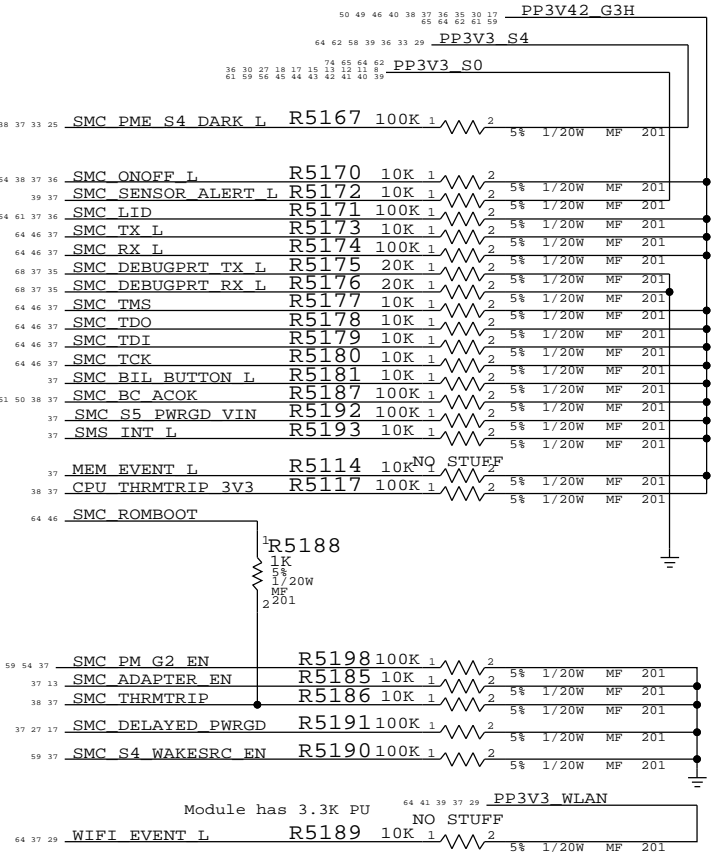
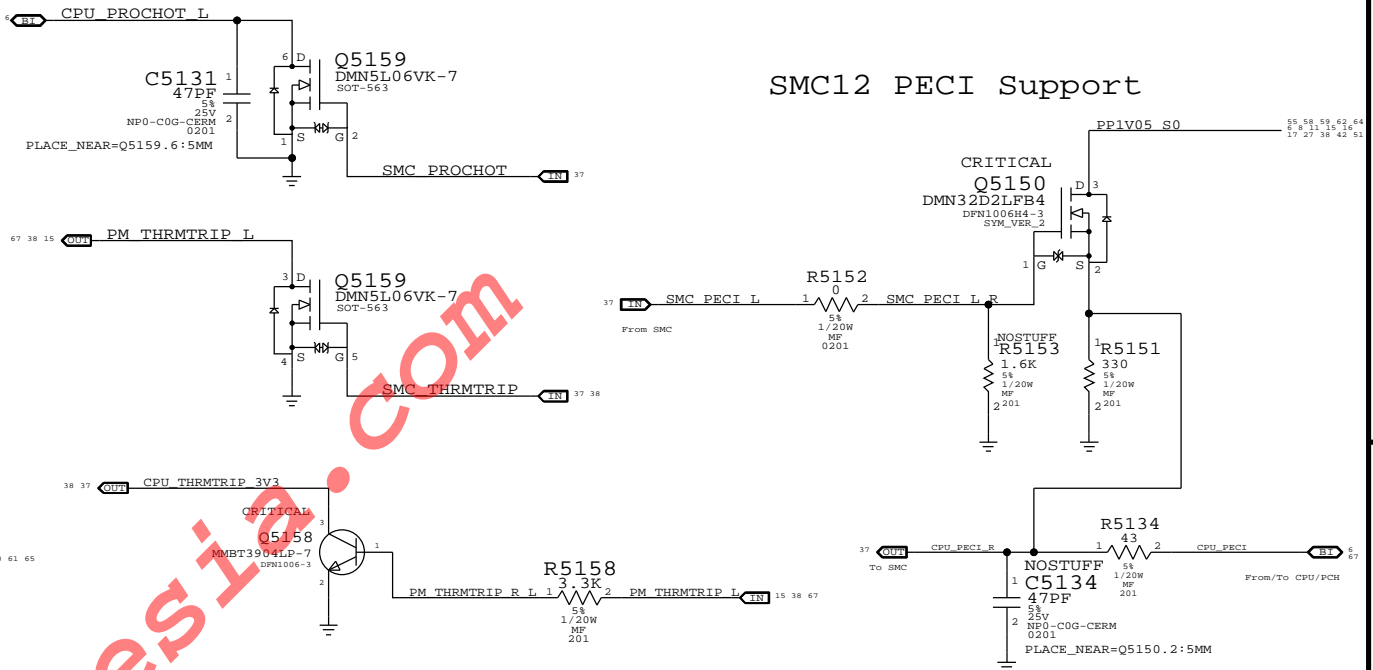



SMC Crystal Circuit

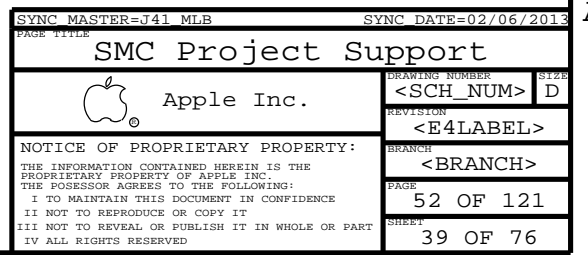
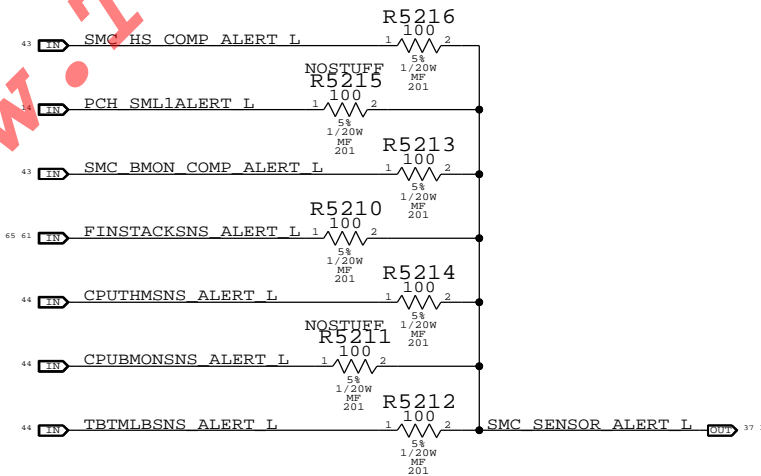
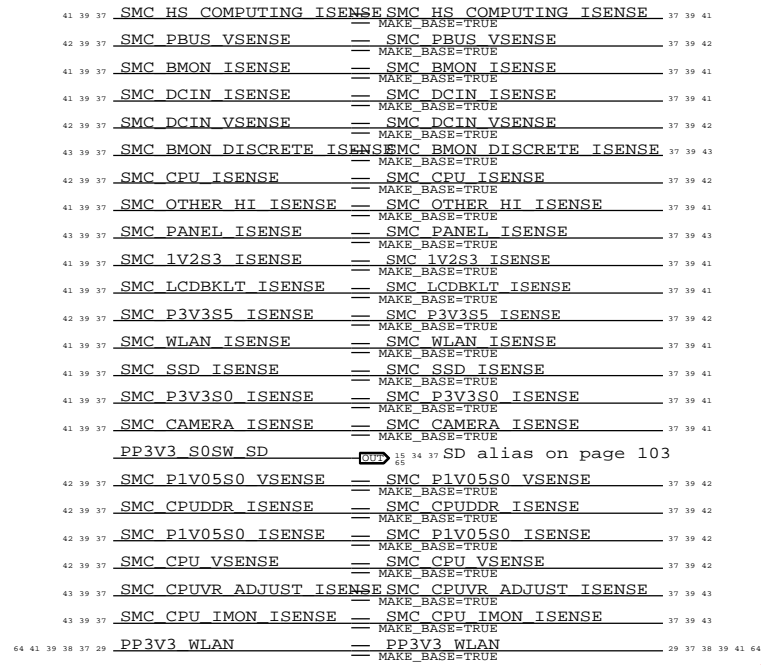
SMC USB Clock require these crystal values: 5,6,8,10,12,16,18,20,24,25 MHz

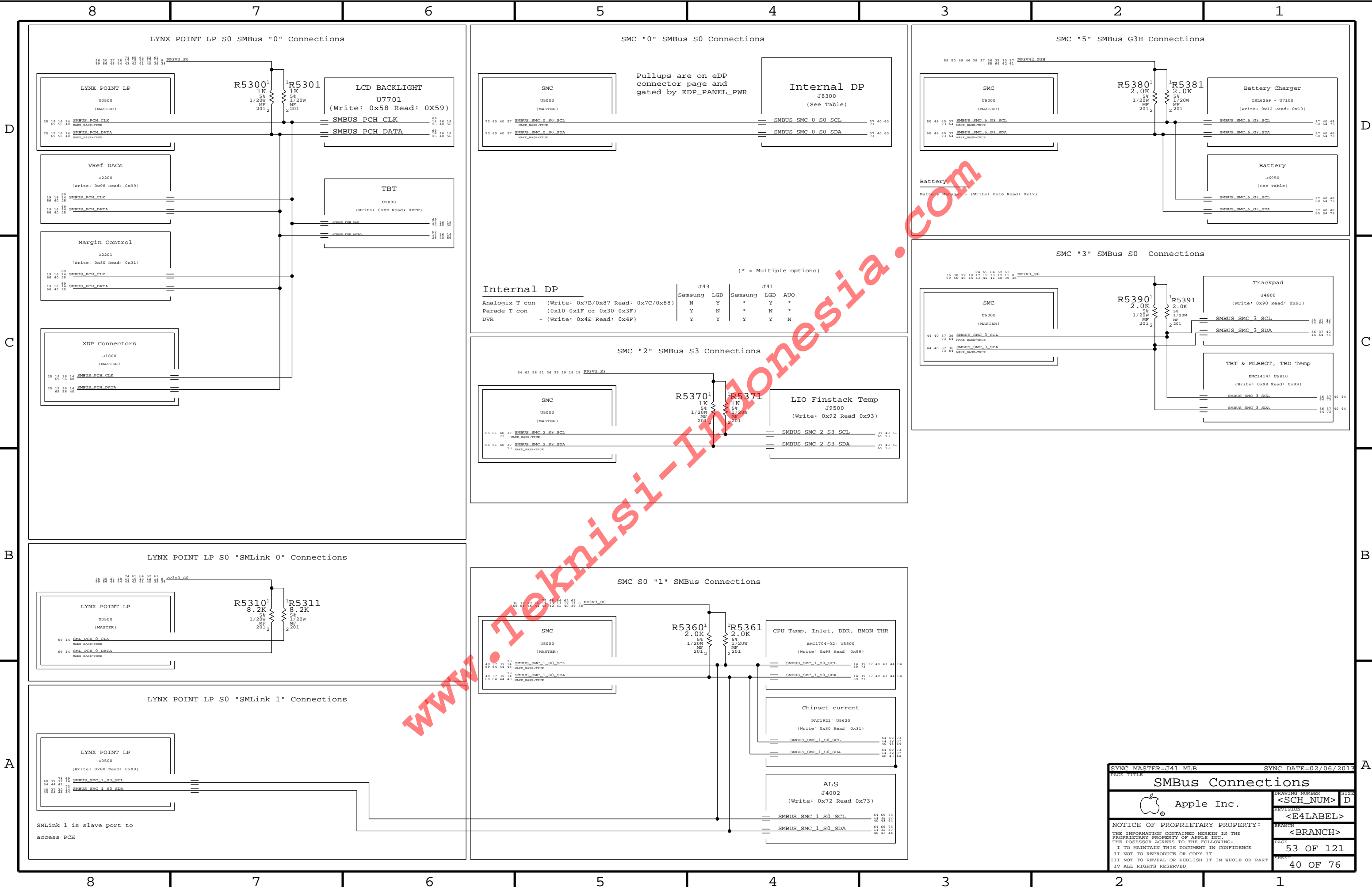


SMC12 PECl Support



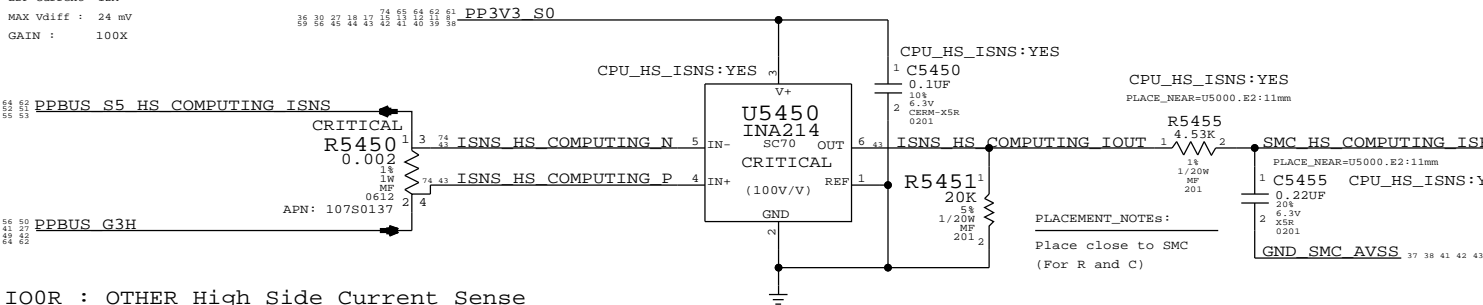
SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
SMC Shared Support			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
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		BRANCH	
		<BRANCH>	
		PAGE	51 OF 121
		SHEET	38 OF 76





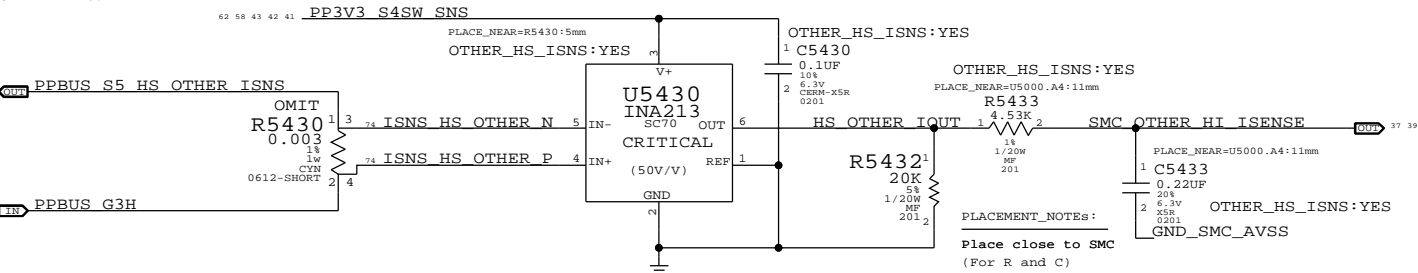
IC0R : COMPUTING High Side Current Sense

```
EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X
```



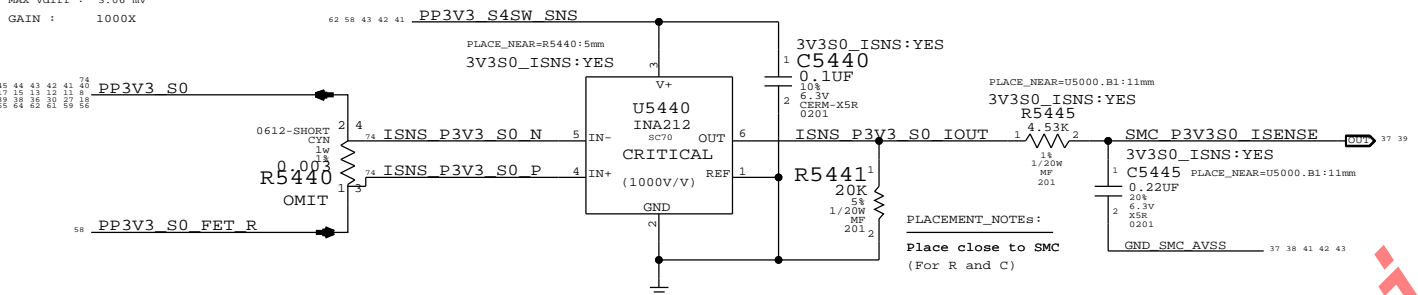
IO0R : OTHER High Side Current Sense

```
EDP Current :10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X
```



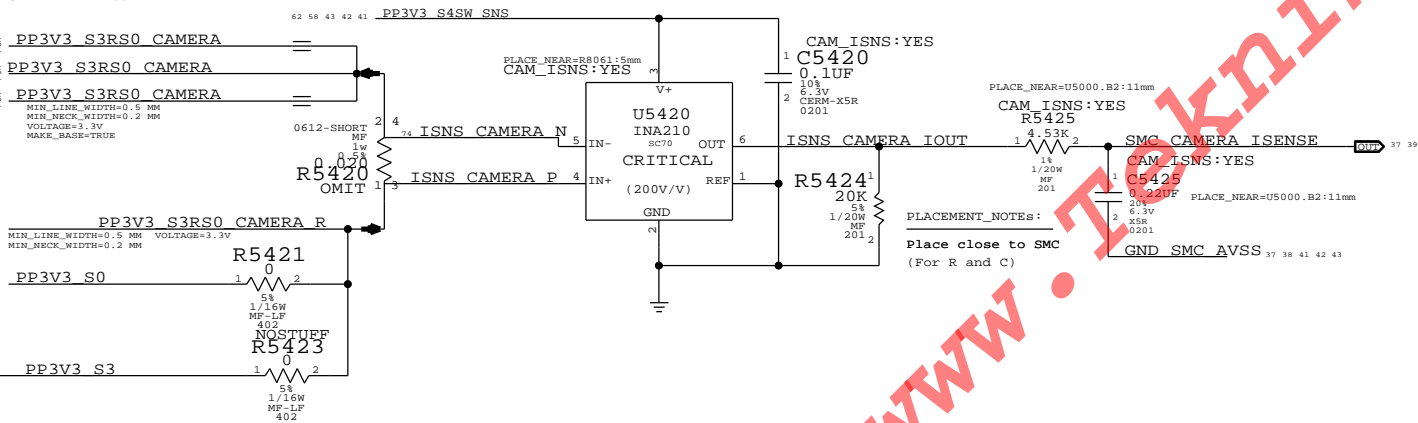
IR0C : 3.3V S0 FET Current Sense

```
EDP Current :1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X
```

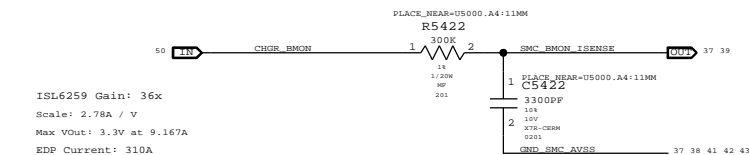


IS2C : 3.3V Camera Current Sense

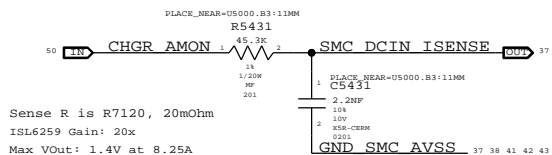
EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X



CHARGER BMON High Side Current Sense

50 

DC-IN (AMON) Current Sense

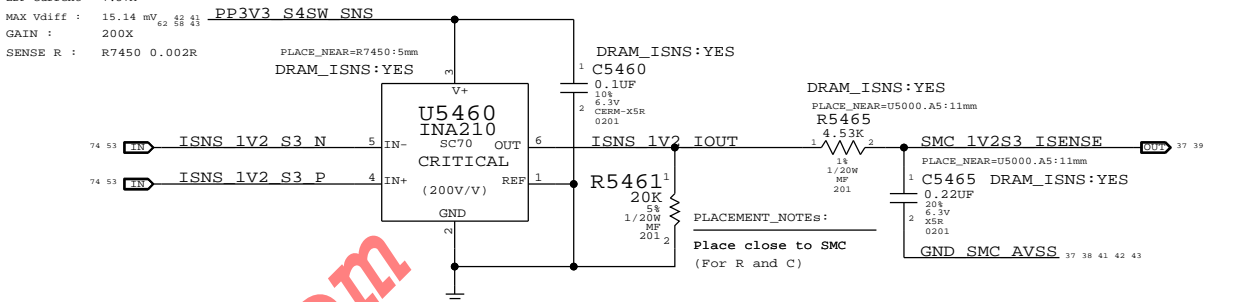


```
Sense R is R7120, 20mOhm
ISL6259 Gain: 20x
Max VOut: 1.4V at 8.25A
Scale: 2.5A / V
EDP Current: 3.5A
```

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.0030HM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

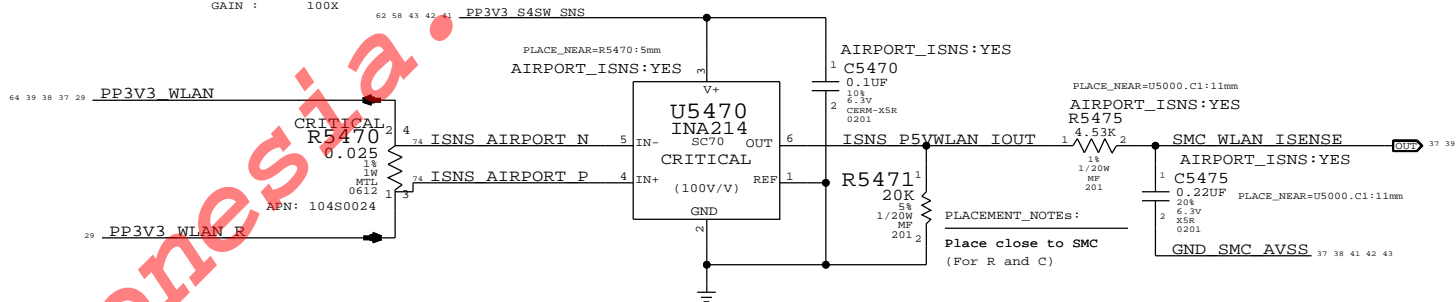
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

```
EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R
```



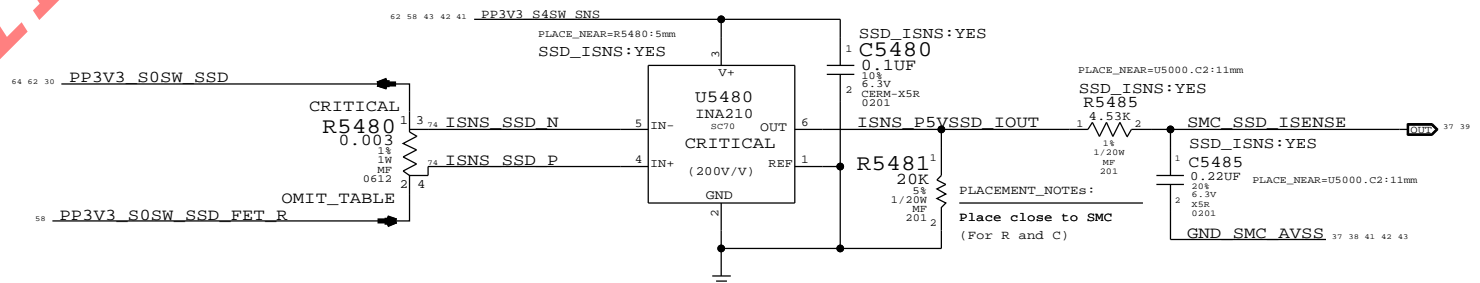
IAPC :AirPort Current Sense

```
EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X
```



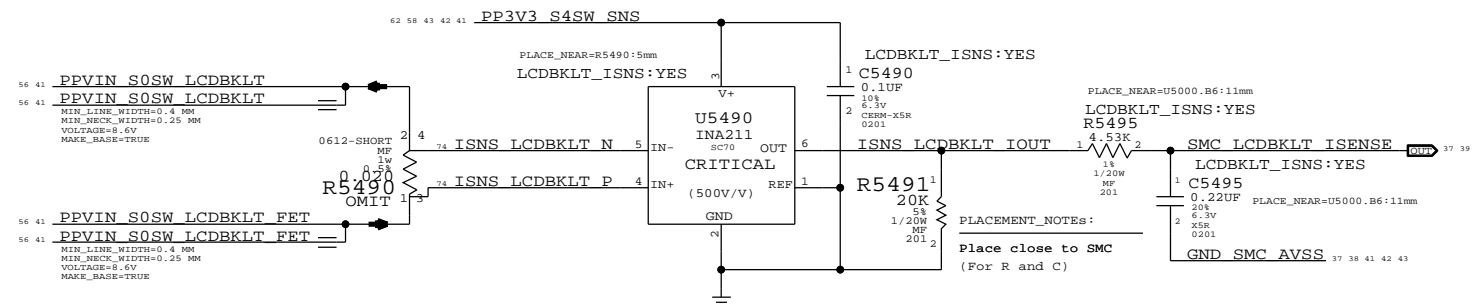
ISDC : SSD Current Sense

```
EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X
```




IBLC : LCD Backlight Driver Input Current Sense

```
EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X
```



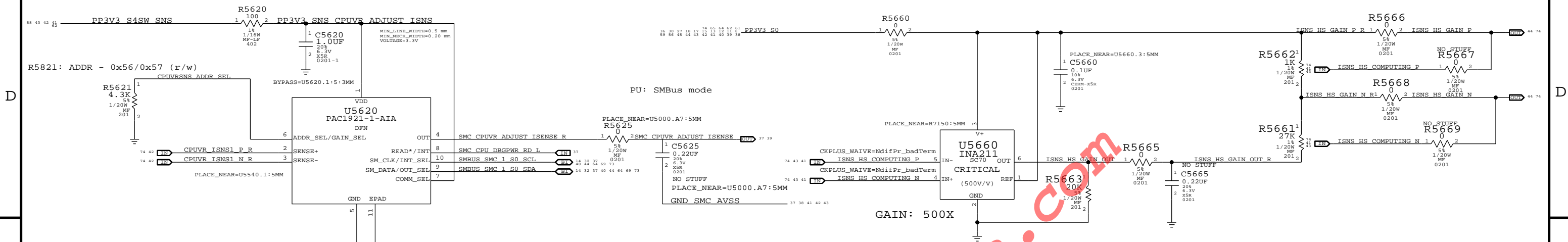
Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCD BKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNCH MASTER=J41 MLB		SYNCH DATE=03/28/2013	
PAGE 1 OF 1			
High Side Current Sensing			
 Apple Inc.		DRAWING NUMBER <SCH_NUM>	
		REVISION <R4LABEL>	
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ICS3 : Adjustable Gain CPU VR Current

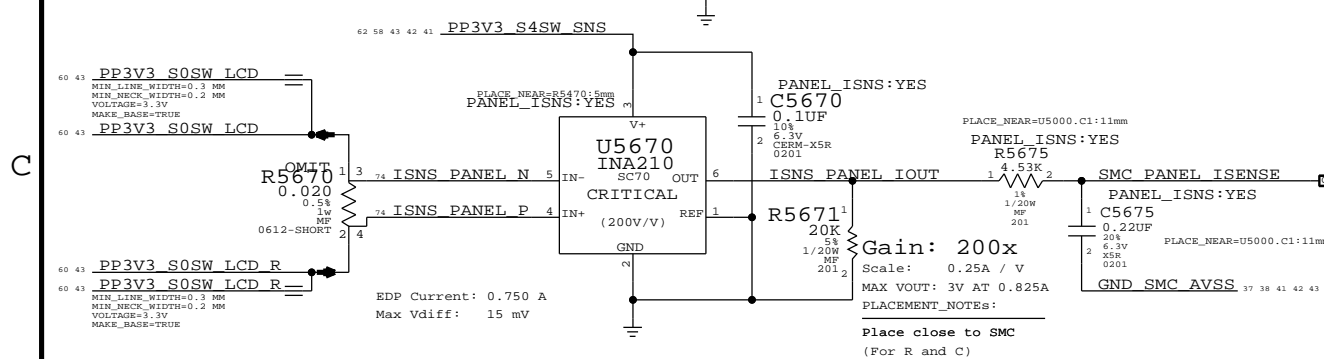
Sense Pins gain stage for U5800 (EMC1704)



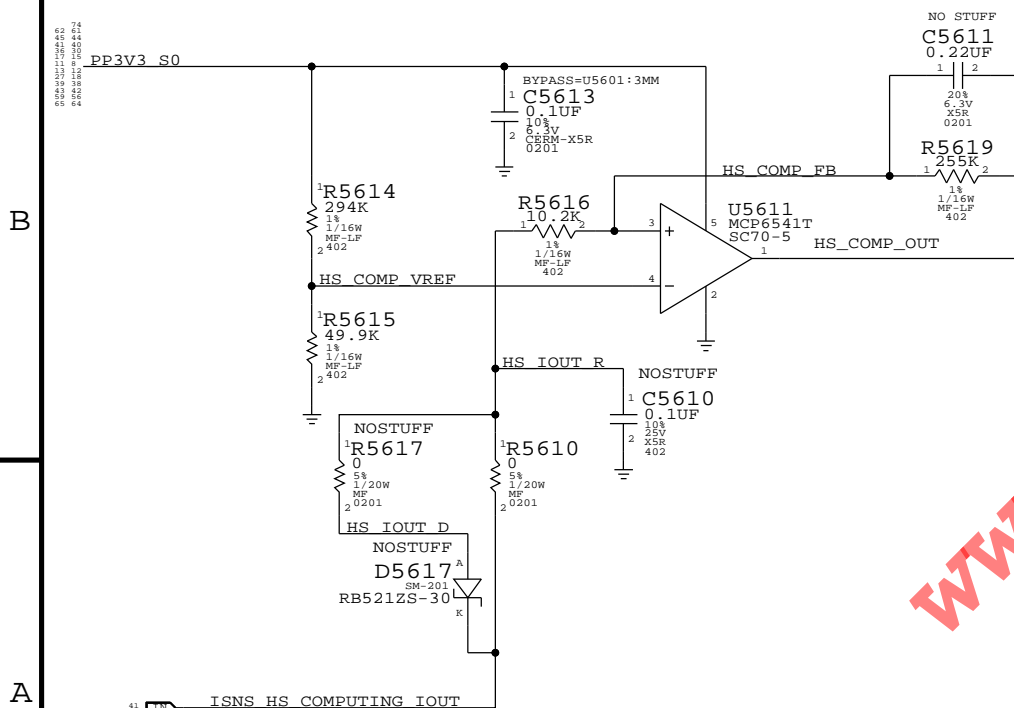
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the minimum current threshold at 0.100mA

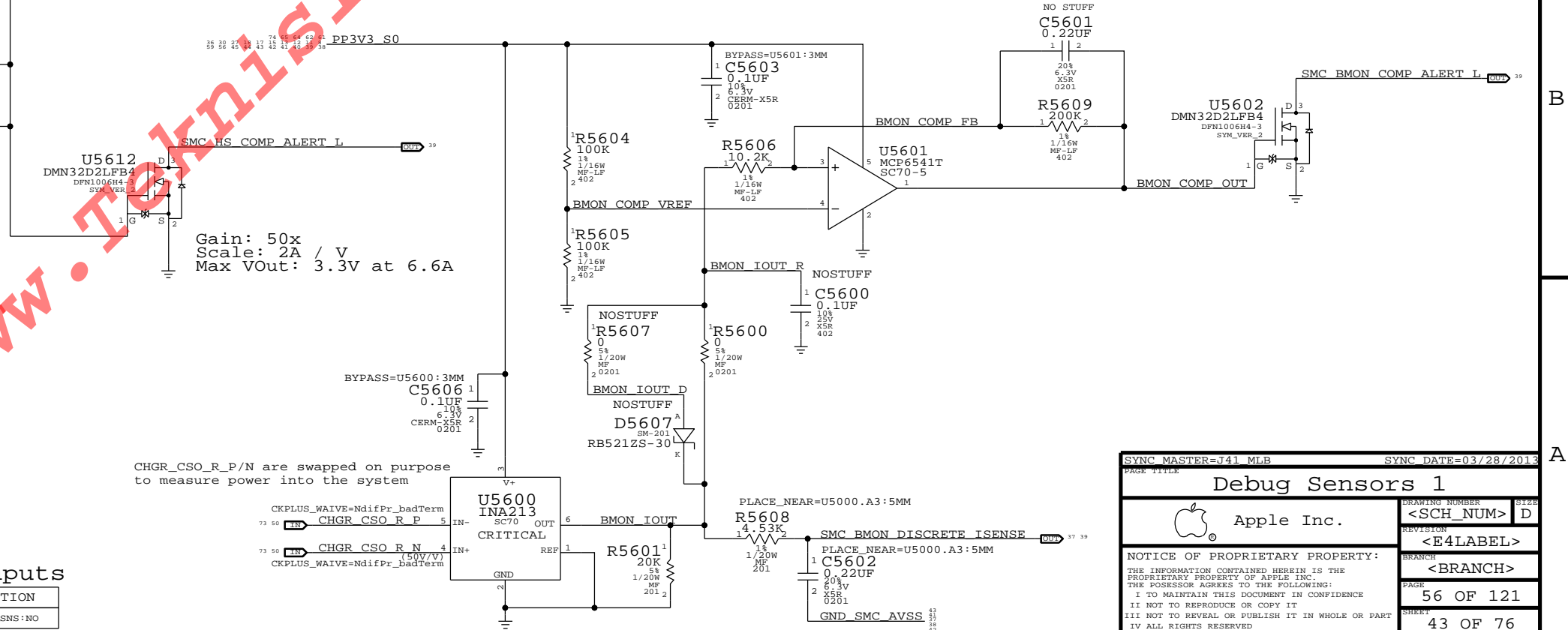
ILDC :LCD Panel Current Sense / Filter



Discrete High side Current threshold



BMON : Discrete BMON Current Sense / Filter



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES, MF, 1/20W, 100K OHM, 5, 0201, SMD	C5675		PANEL_ISNS:NO

SYNC MASTER=J41 MLB

SYNC DATE=03/28/2013

Debug Sensors 1

Apple Inc.

Apple Inc.

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DRAWING NUMBER

<SCH_NUM>

REVISION

<E4LABEL>

BRANCH

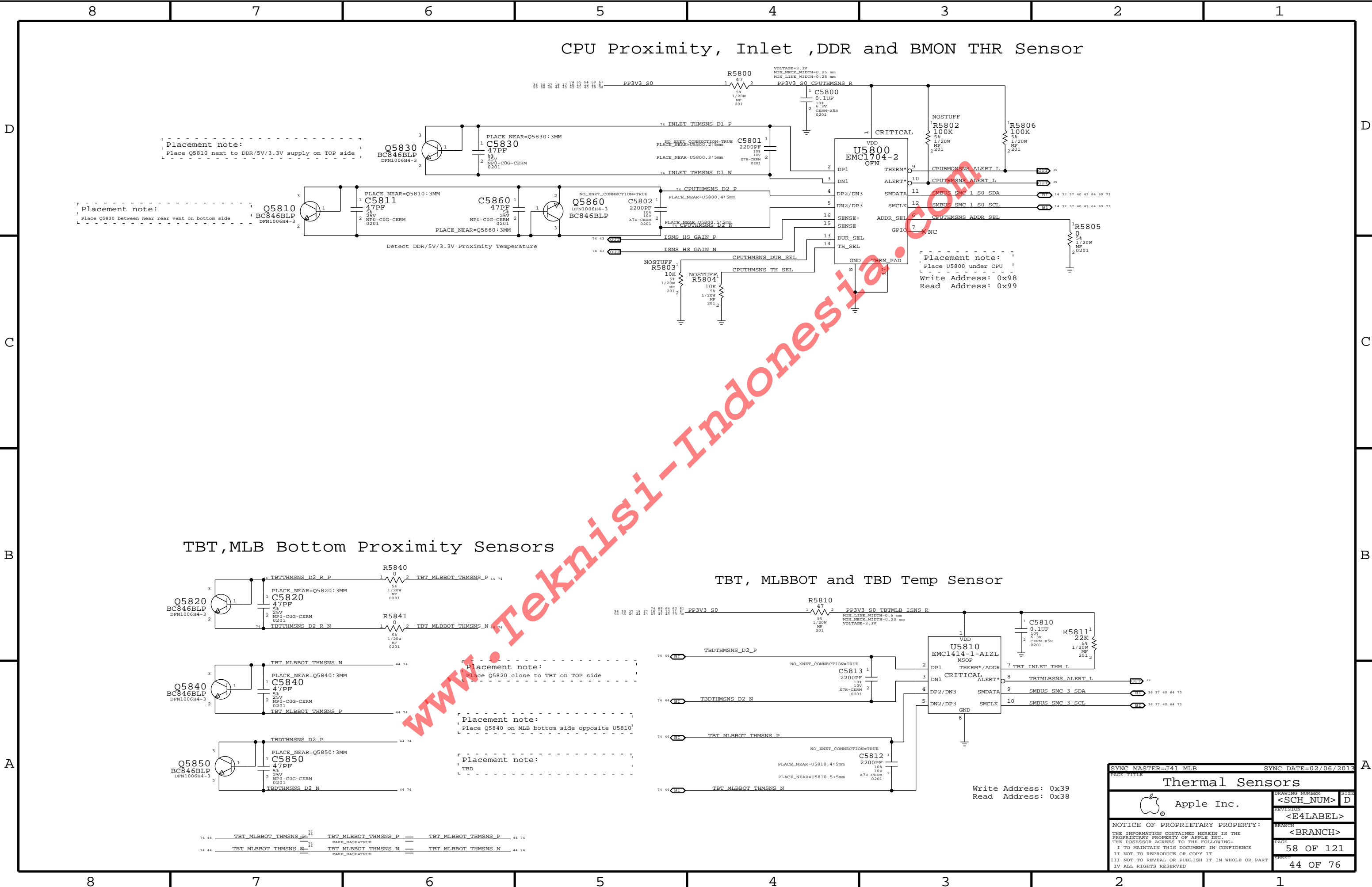
<BRANCH>

PAGE

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SHEET

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CPU Proximity, Inlet ,DDR and BMON THR Sensor

Placement note:
Place Q5810 next to DDR/5V/3.3V supply on TOP side

Placement note:
Place Q5830 between rear vent on bottom side

Placement note:
Place U5800 under CPU
Write Address: 0x98
Read Address: 0x99

TBT,MLB Bottom Proximity Sensors

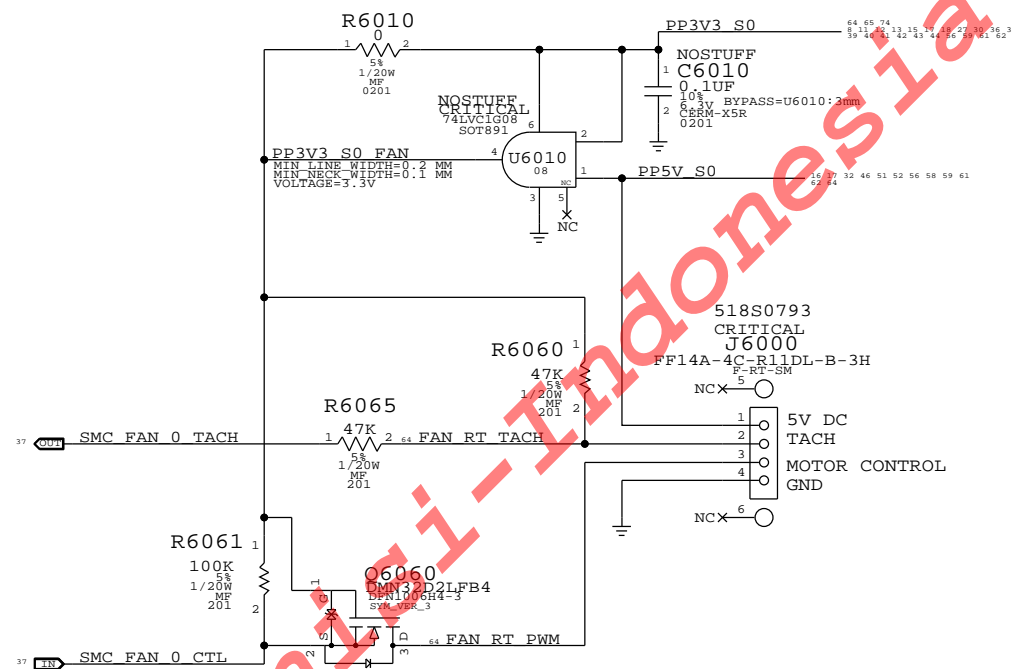
TBT, MLBBOT and TBD Temp Sensor

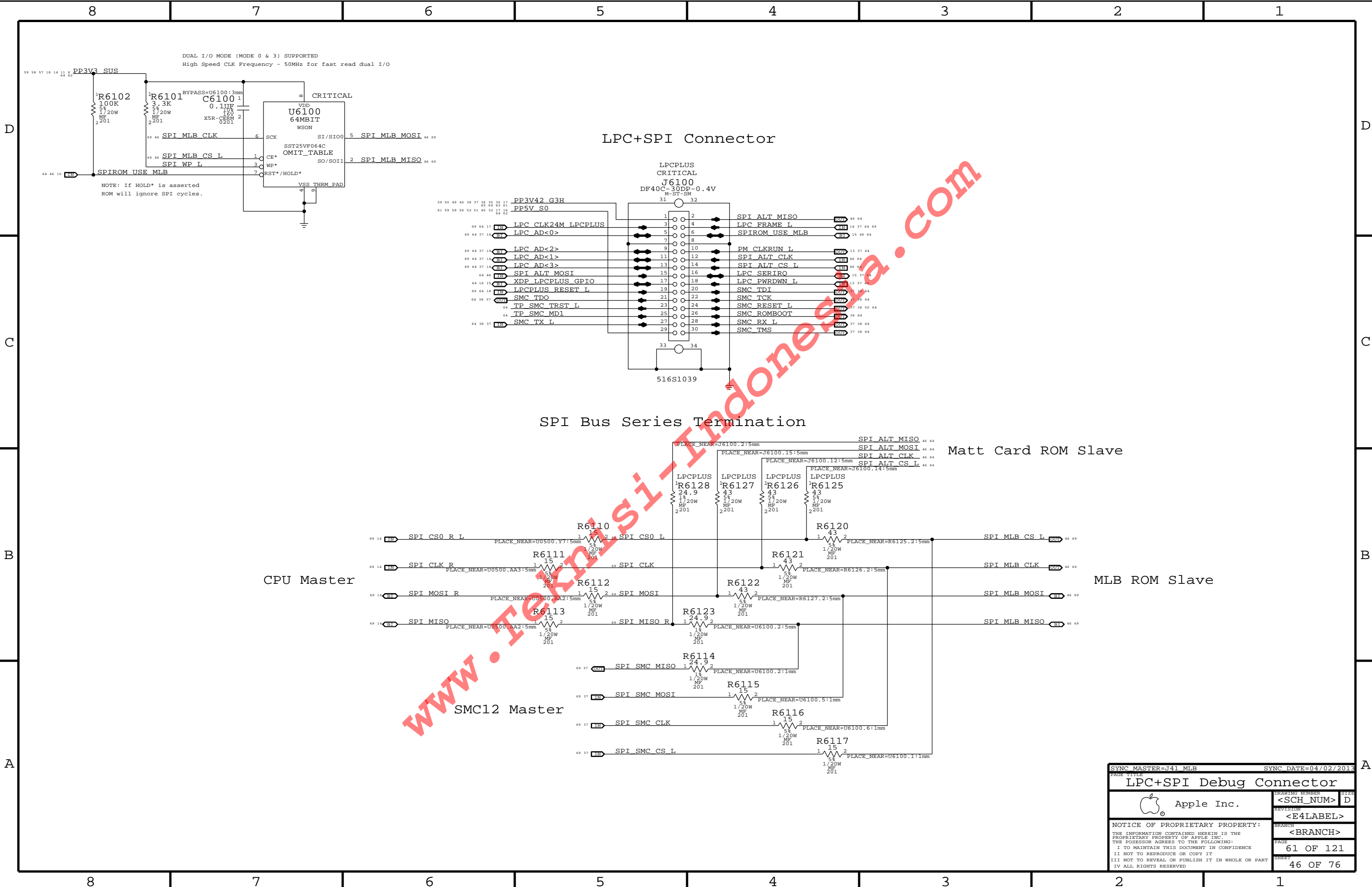
Placement note:
Place Q5820 close to TBT on TOP side

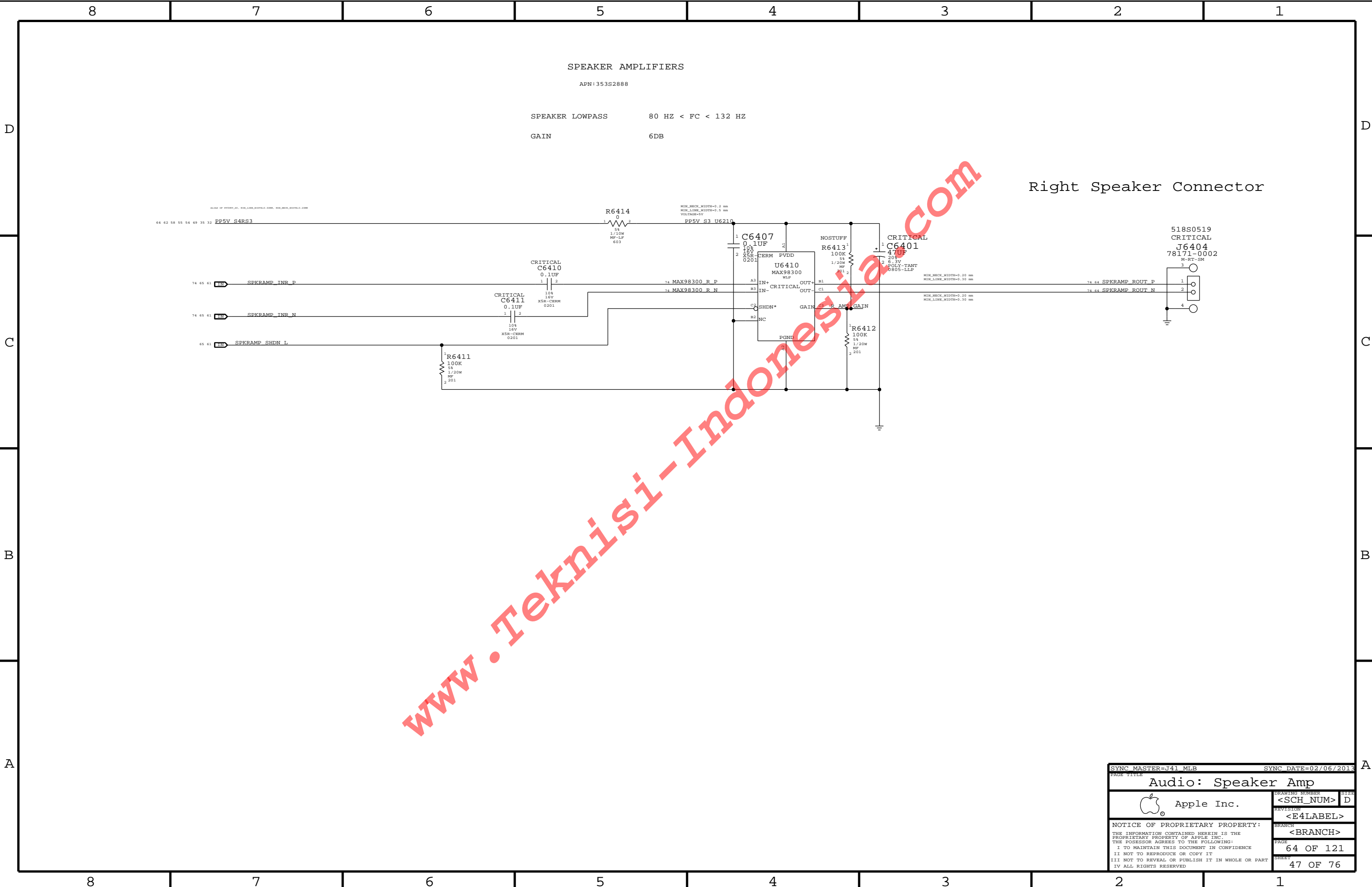
Placement note:
Place Q5840 on MLB bottom side opposite U5810

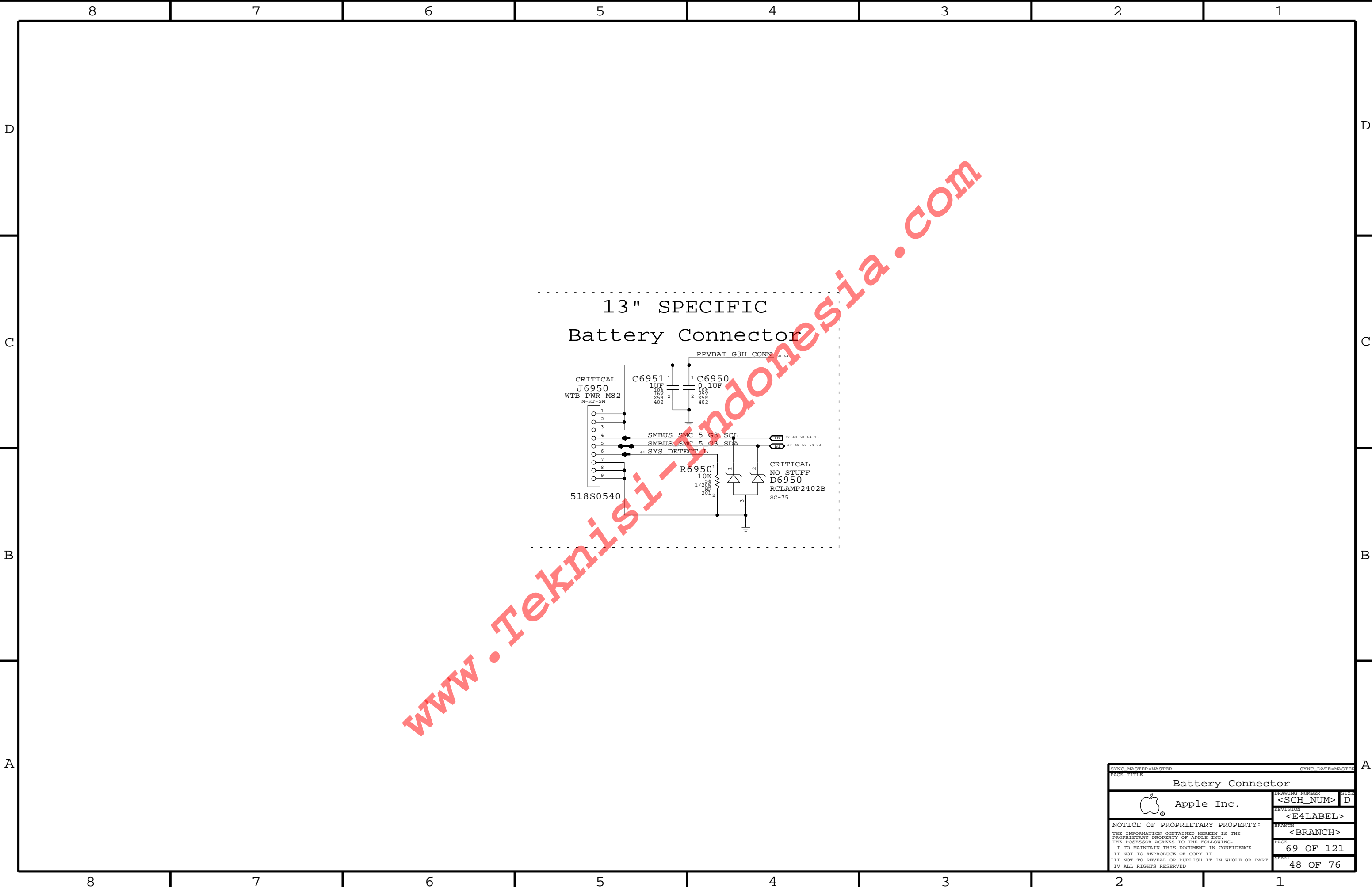
Placement note:
TBD


SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE		Thermal Sensors	
Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	58 OF 121
		SHEET	44 OF 76
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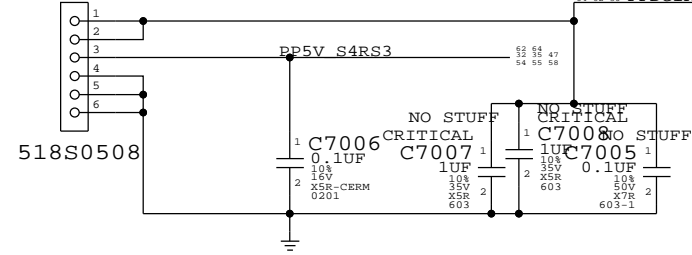




SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Battery Connector			
	DRAWING NUMBER		SIZE
	<SCH_NUM>		D
Apple Inc.	REVISION		
	<E4LABEL>		
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		PAGE	69 OF 121
		SHEET	48 OF 76

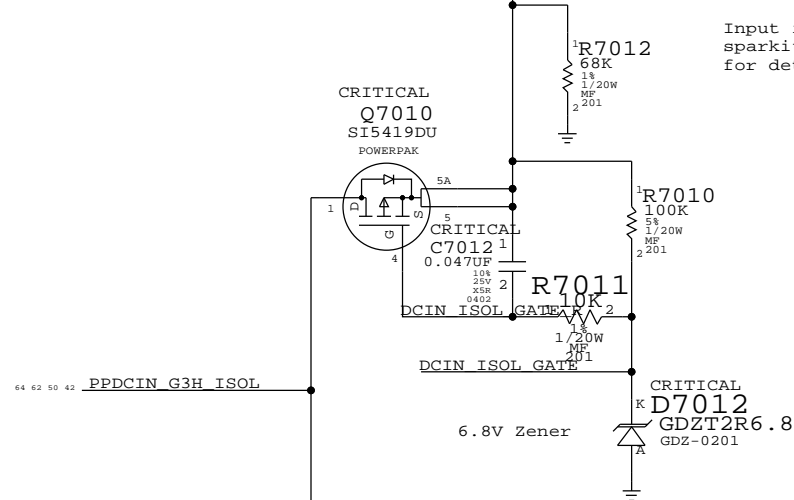
MLB to LIO Power Cable Connector

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM



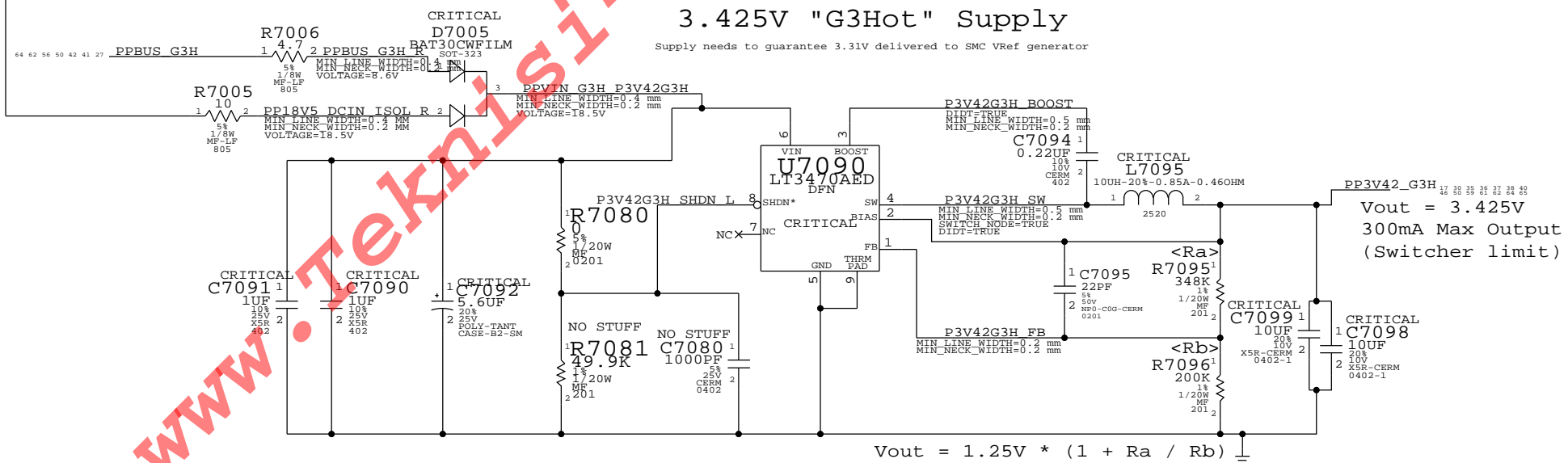
Input impedance of 68K meets
sparkiterture requirements
for detection of B121 (16.5V)

CRITICAL
Q7010
SI5419DU
POWERPAK




3.425V "G3Hot" Supply

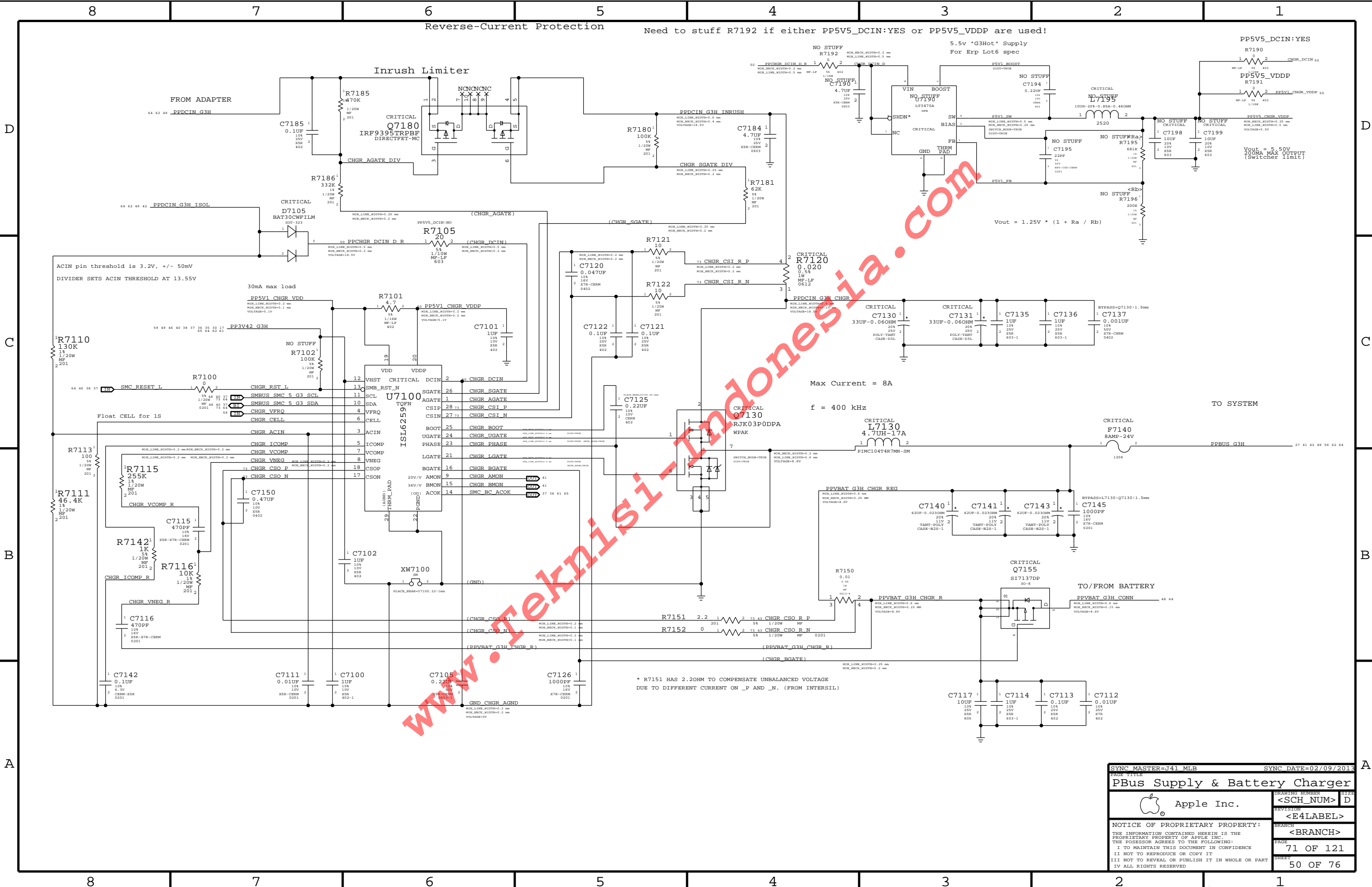
Supply needs to guarantee 3.31V delivered to SMC VRef generator




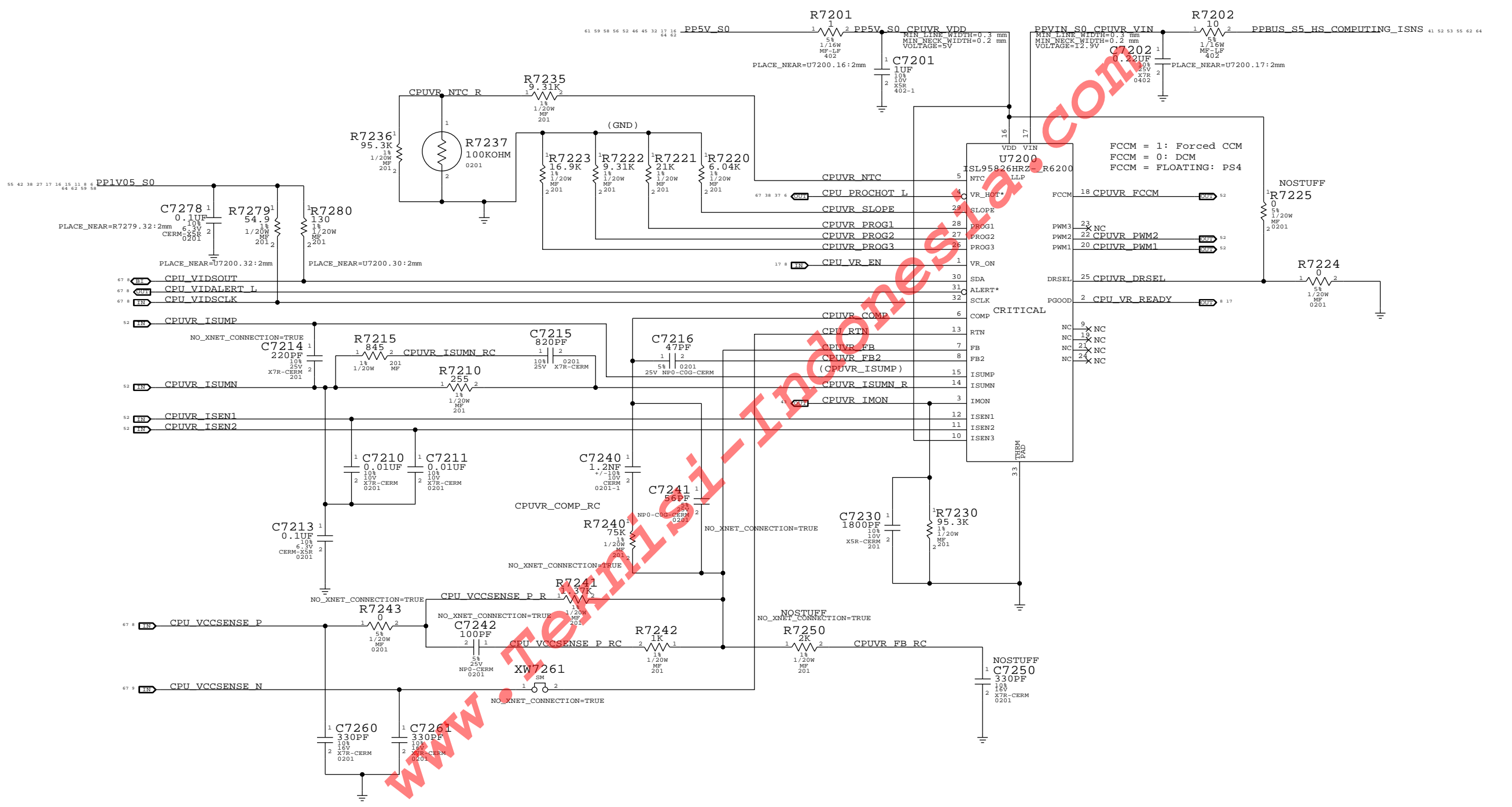
Vout = 3.425V
300mA Max Output
(Switcher limit)


$$V_{out} = 1.25V * (1 + R_a / R_b)$$

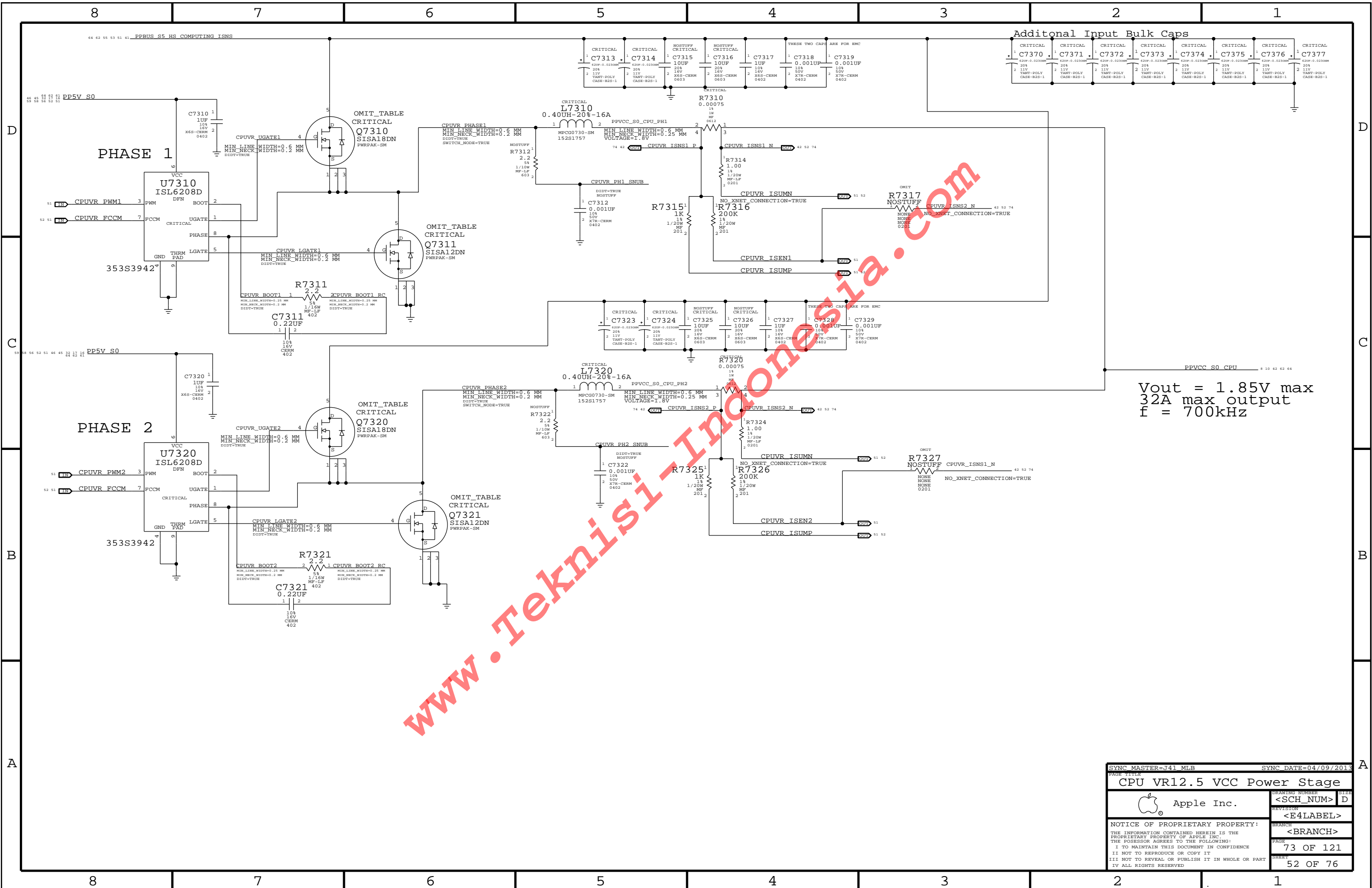
SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
DC-In & G3H Supply			
 Apple Inc.	DRAWING NUMBER	SIZE	
	<SCH_NUM>	D	
	REVISION		
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	BRANCH		
	<BRANCH>		
	PAGE	70 OF 121	
	SHEET	49 OF 76	




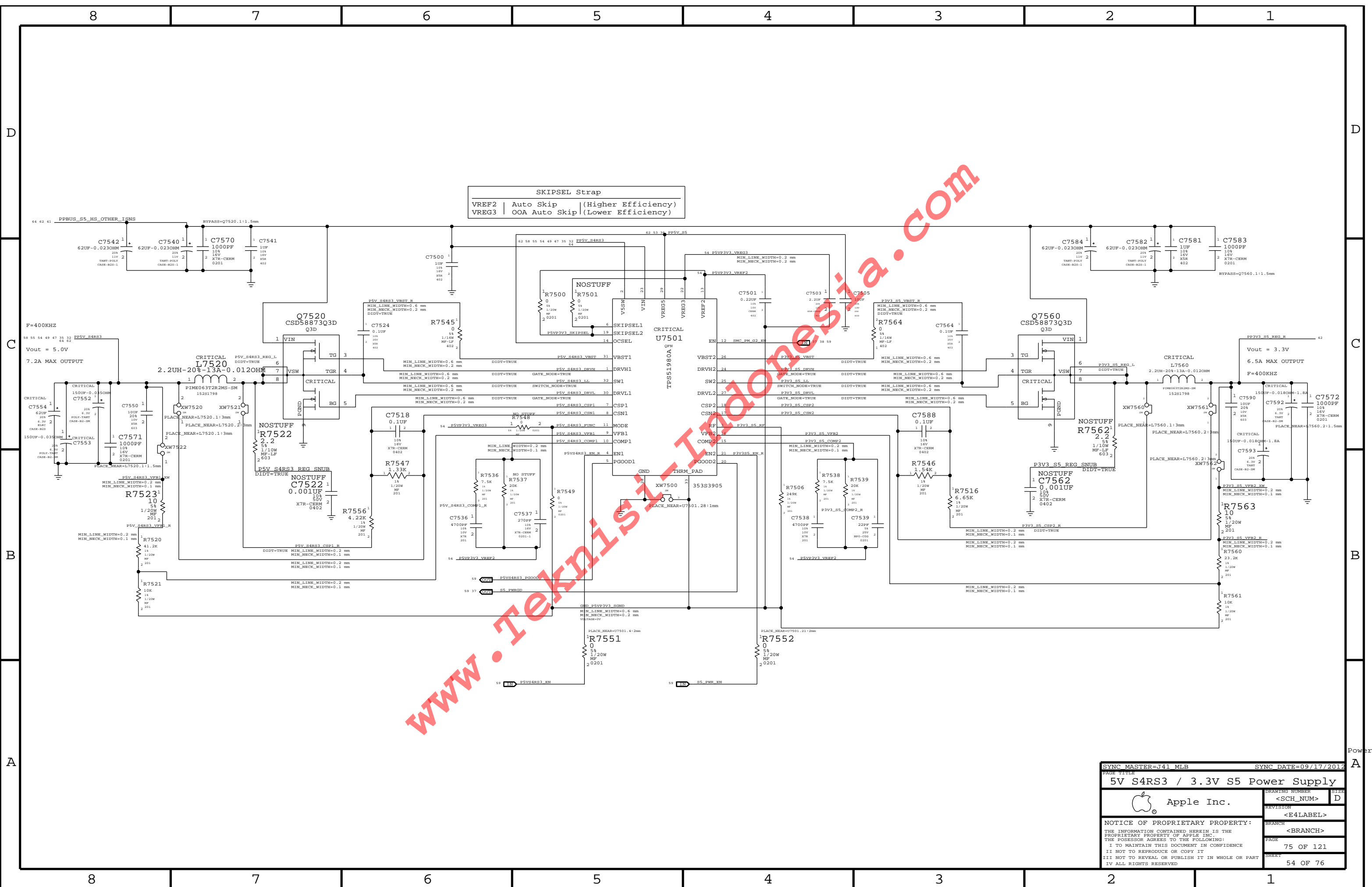
SYNC MASTER=J41 MLB		SYNC DATE=02/09/2013		
PAGE TITLE				
PBus Supply & Battery Charger				
	DRAWING NUMBER		SIZE	
	<SCH_NUM>		D	
	REVISION			
<E4LABEL>				
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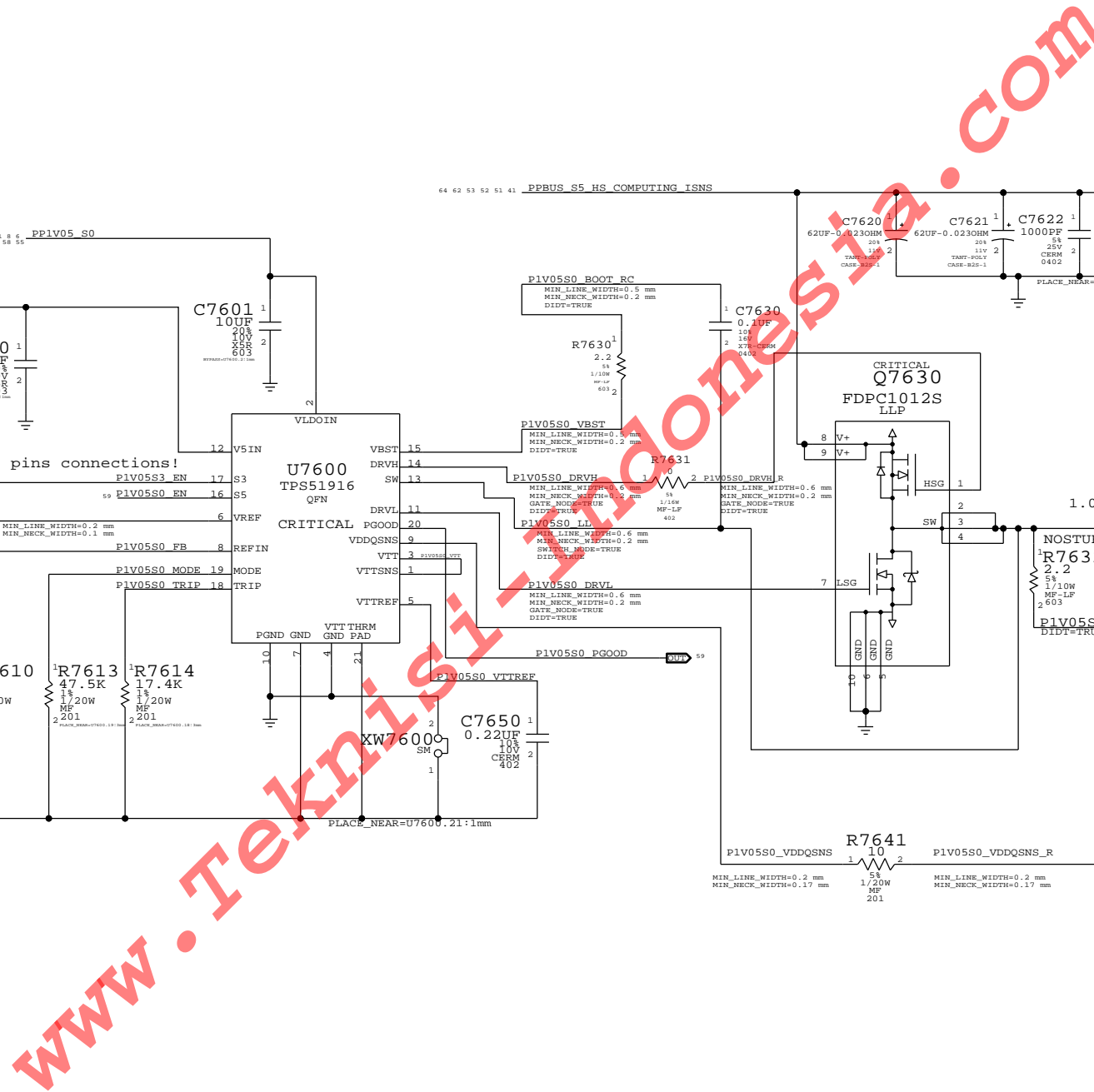


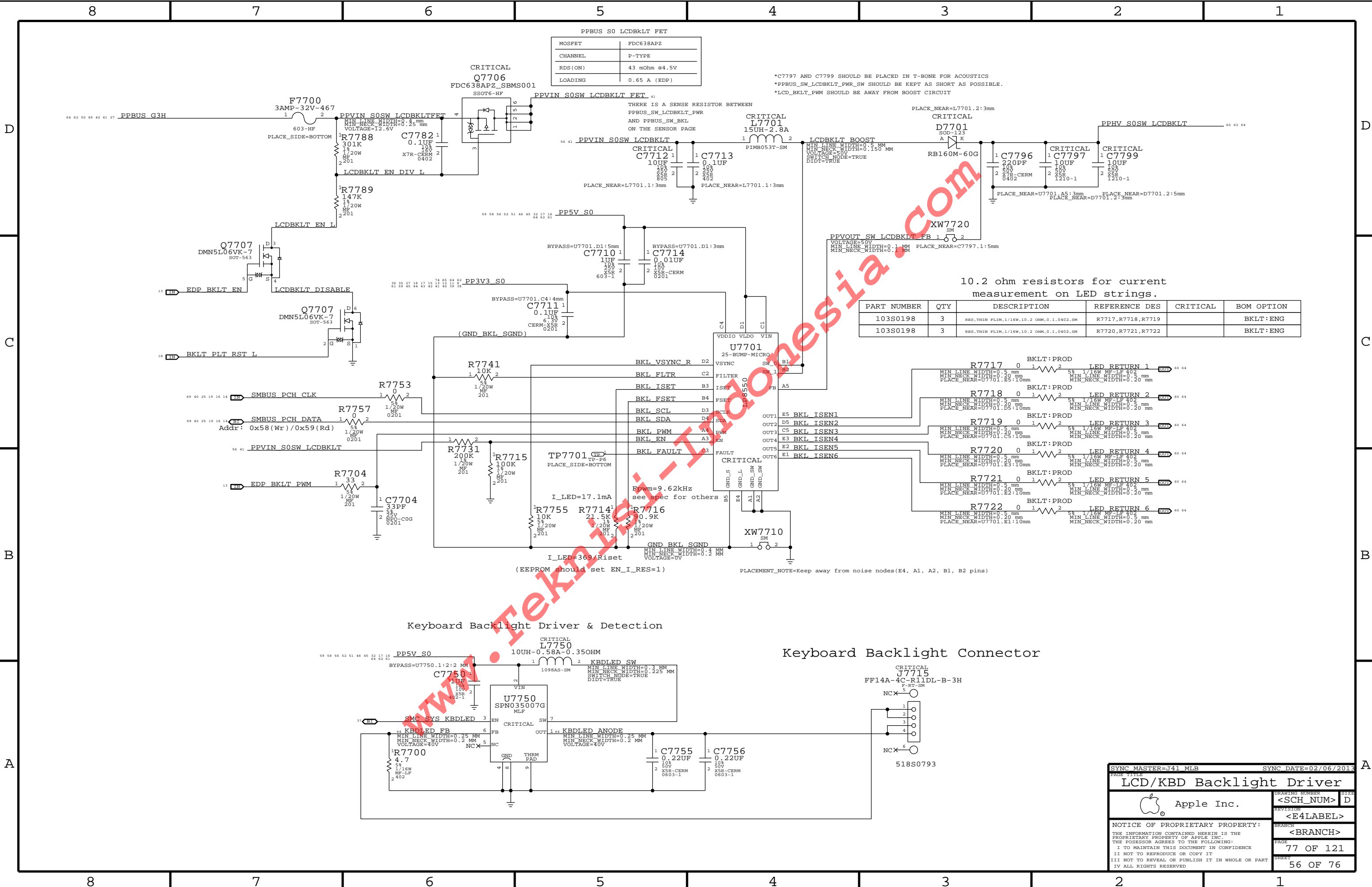
SYNC MASTER=J41 MLB		SYNC DATE=04/09/2013	
PAGE TITLE			
CPU VR12.6 VCC Regulator IC			
 Apple Inc.		DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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SYNC MASTER=J41 MLB		SYNC DATE=04/09/2013	
PAGE TITLE			
CPU VR12.5 VCC Power Stage			
		Apple Inc.	
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		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
		BRANCH	
		<BRANCH>	
		PAGE	73 OF 121
		SHEET	52 OF 76







PPBUS SW LCDBKLT FET	
MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)

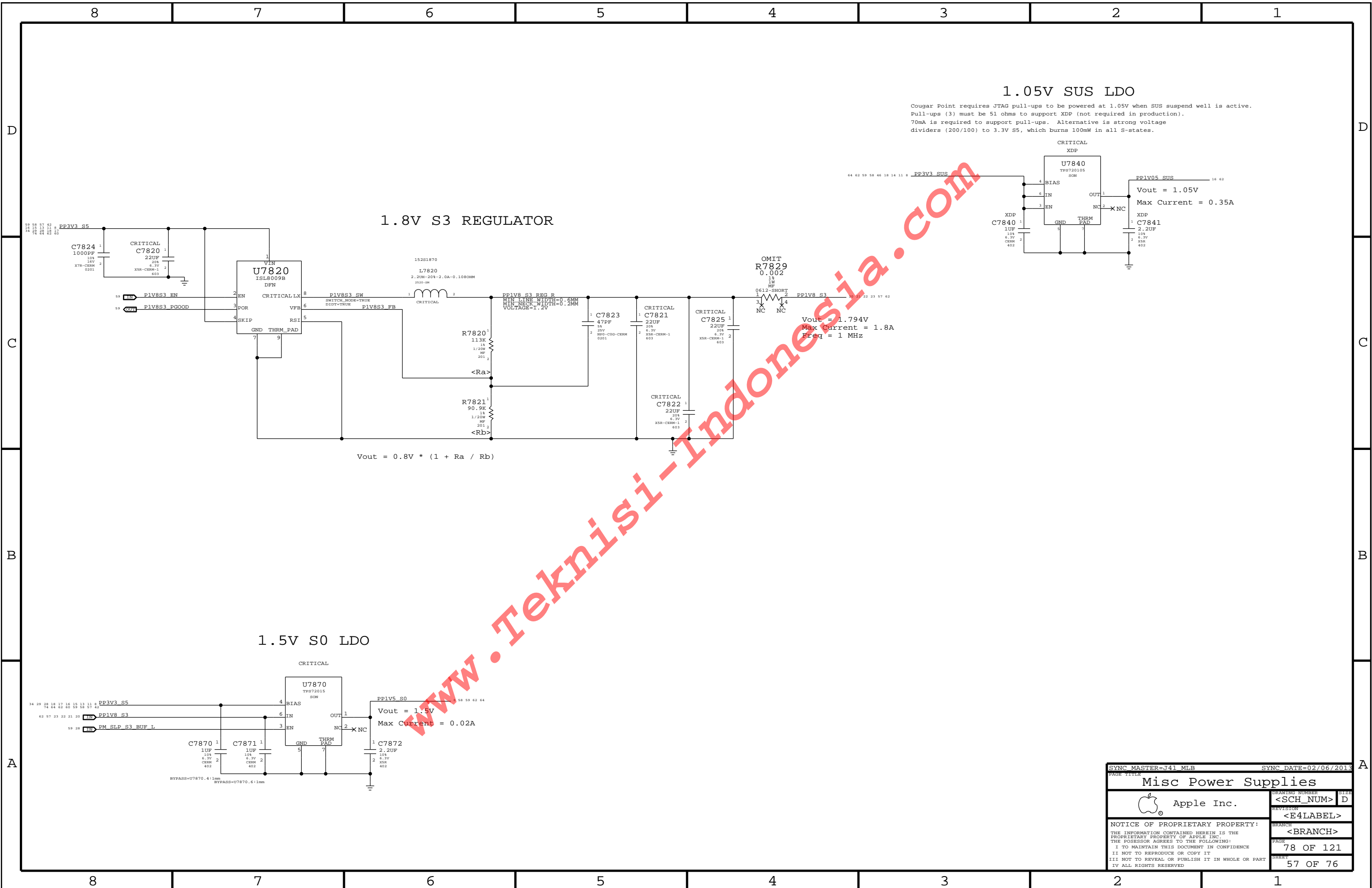
*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

Keyboard Backlight Driver & Detection

Keyboard Backlight Connector

SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE		LCD/KBD Backlight Driver	
DRAWING NUMBER		<SCH_NUM>	SIZE D
REVISION		<E4LABEL>	BRANCH
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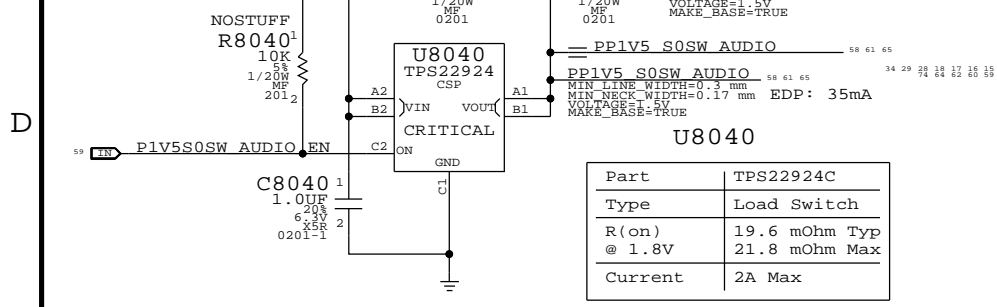


8	7	6	5	4	3	2	1
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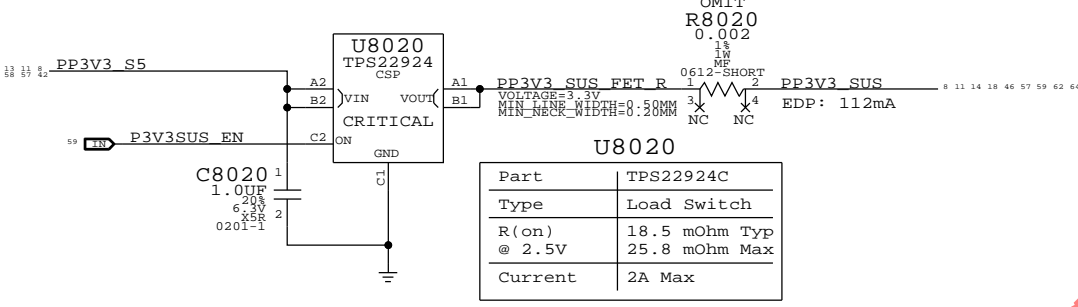
1.5V S0 Audio Switch

Loading specs per J41/43_PowerBudget_Riviera_rev0.99e

3.3V SUS Switch

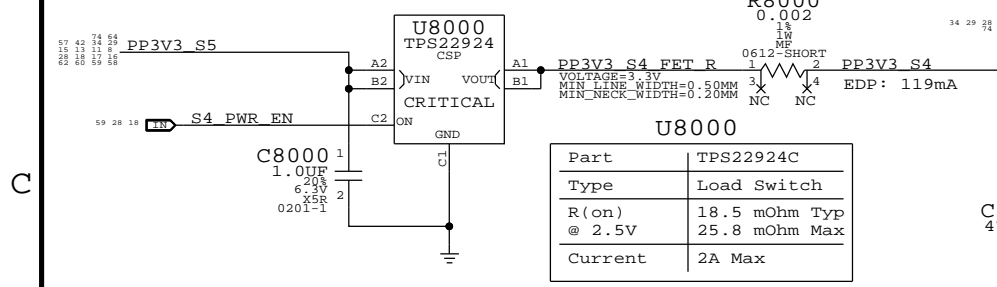


Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max



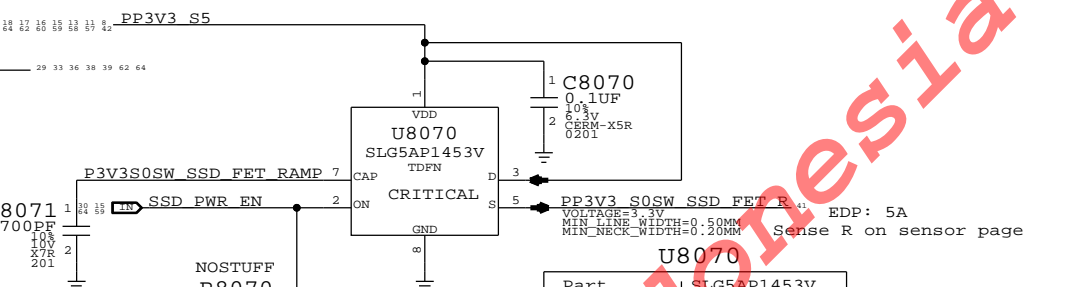
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V S4 Switch OMIT
P9000



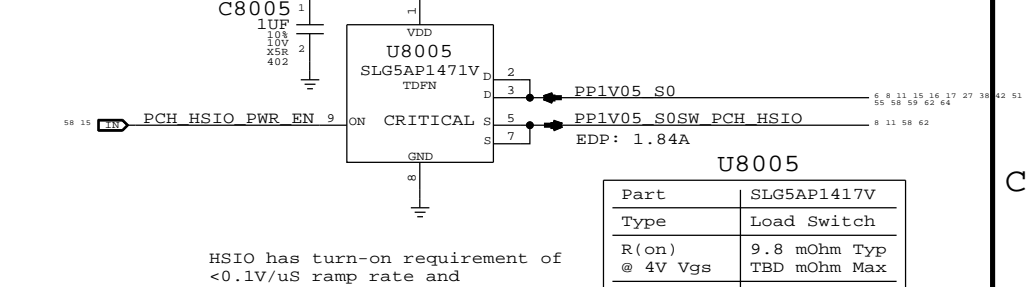
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V S4 Switch



Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25°C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

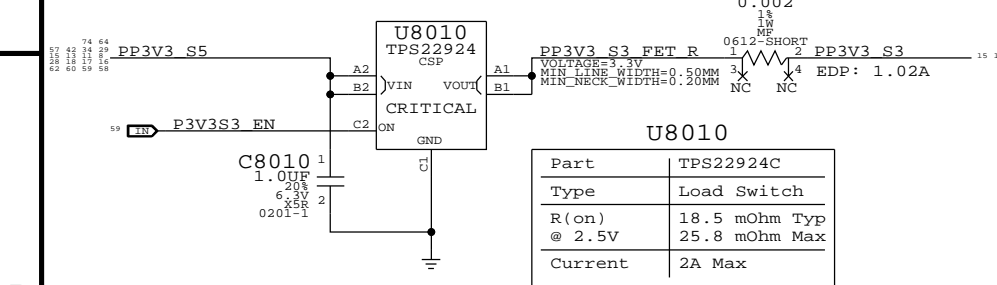
3.3V S4 Switch



Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

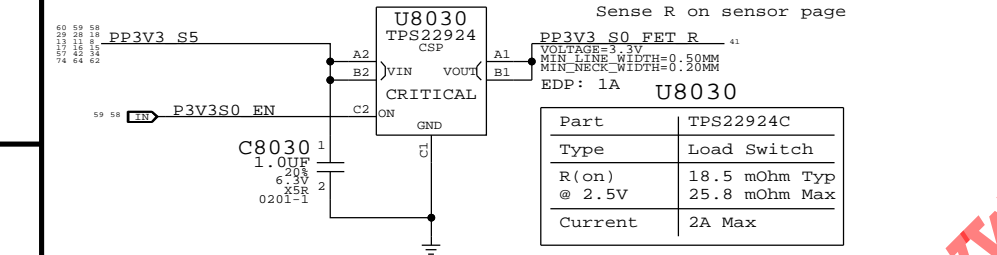
HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

3.3V S3 Switch OMIT
R8011



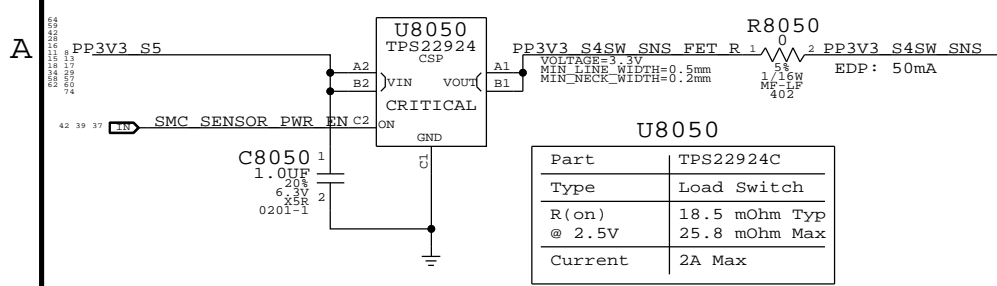
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

```
3.3V S0 Switch
```



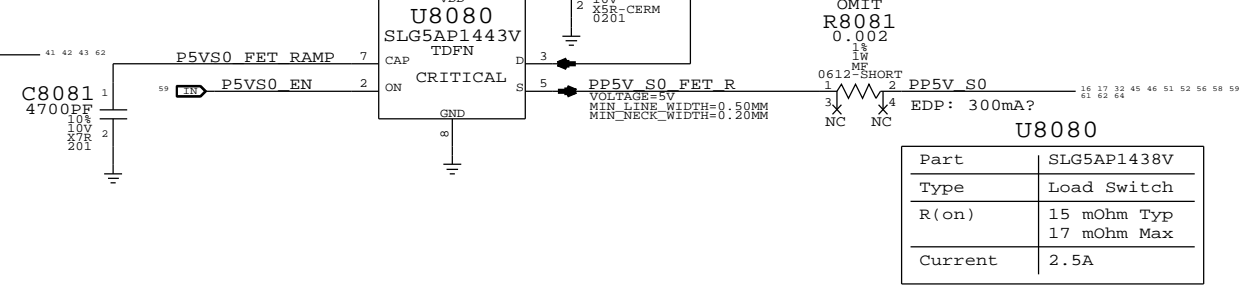
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

3.3V Sensor Switch

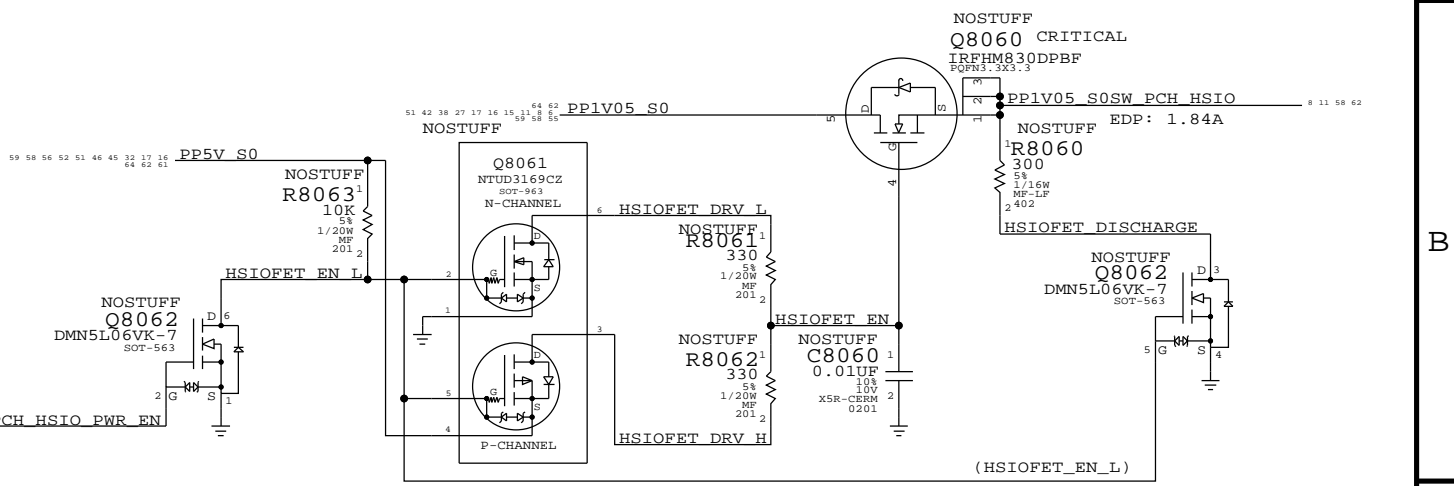


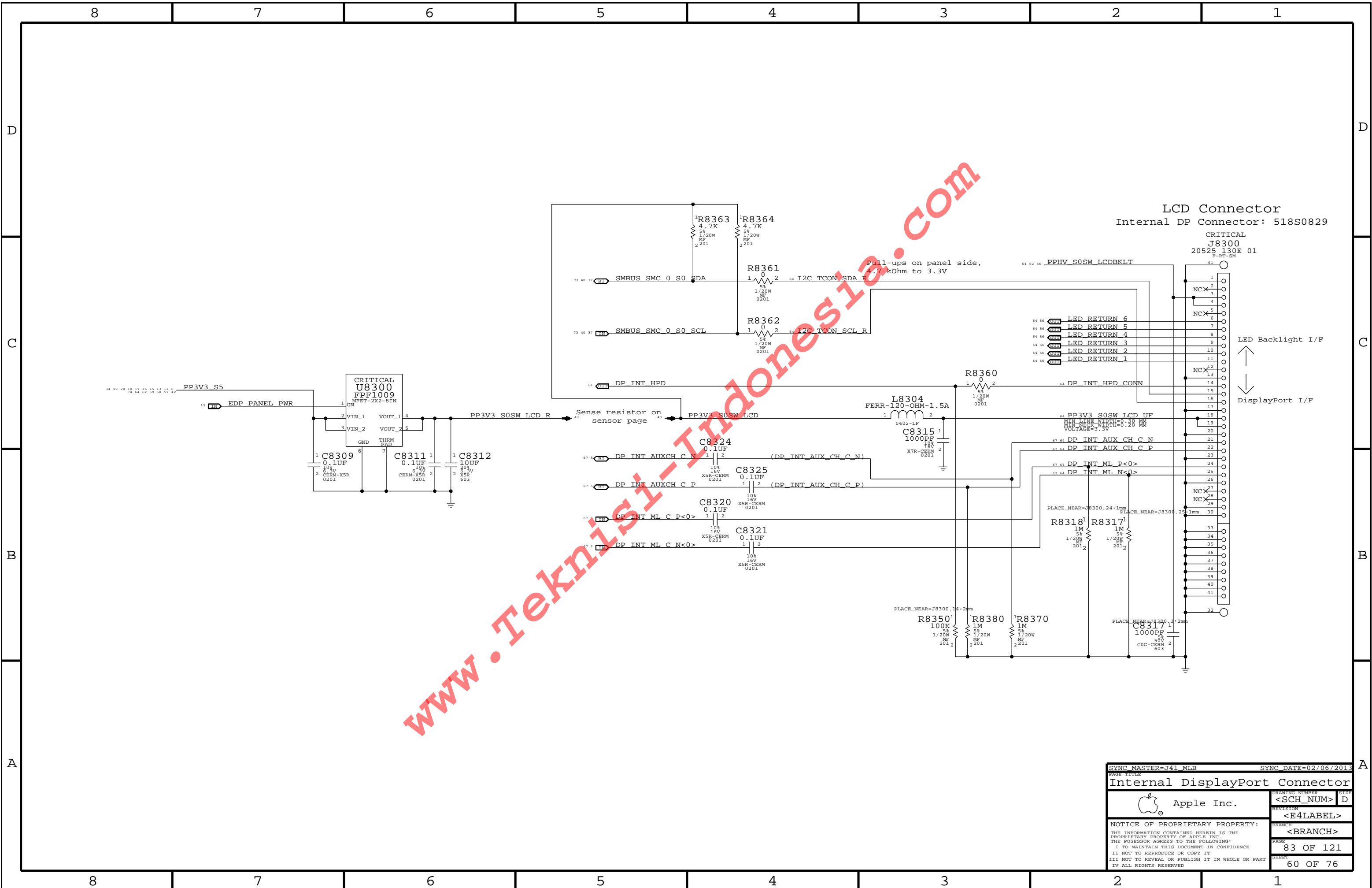
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max


3.3V Sensor Switch

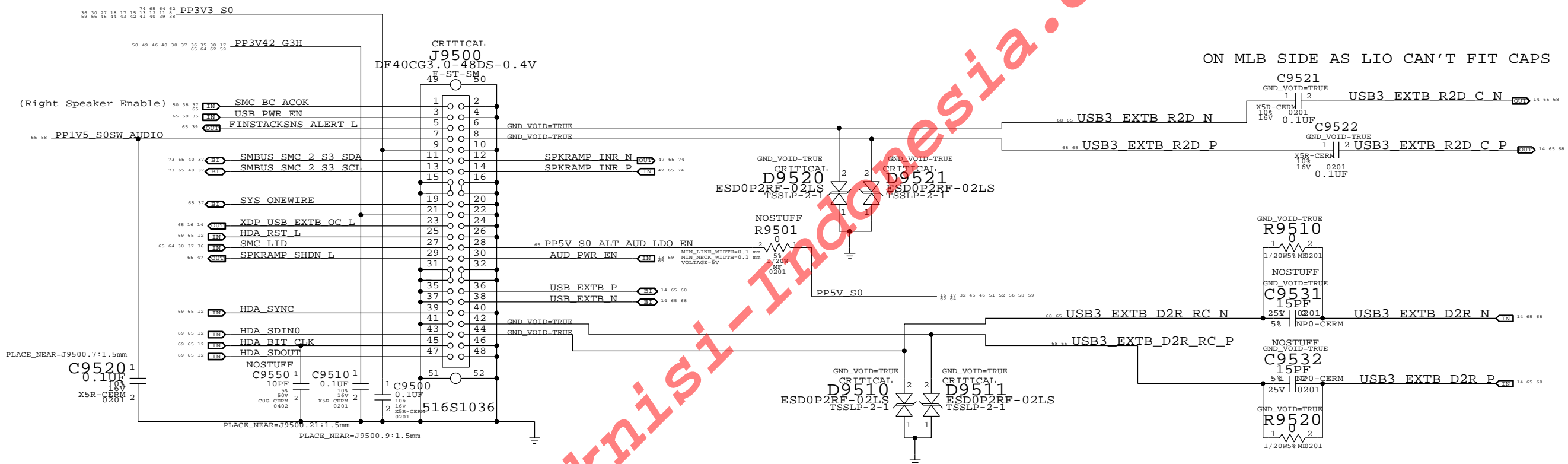



Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A

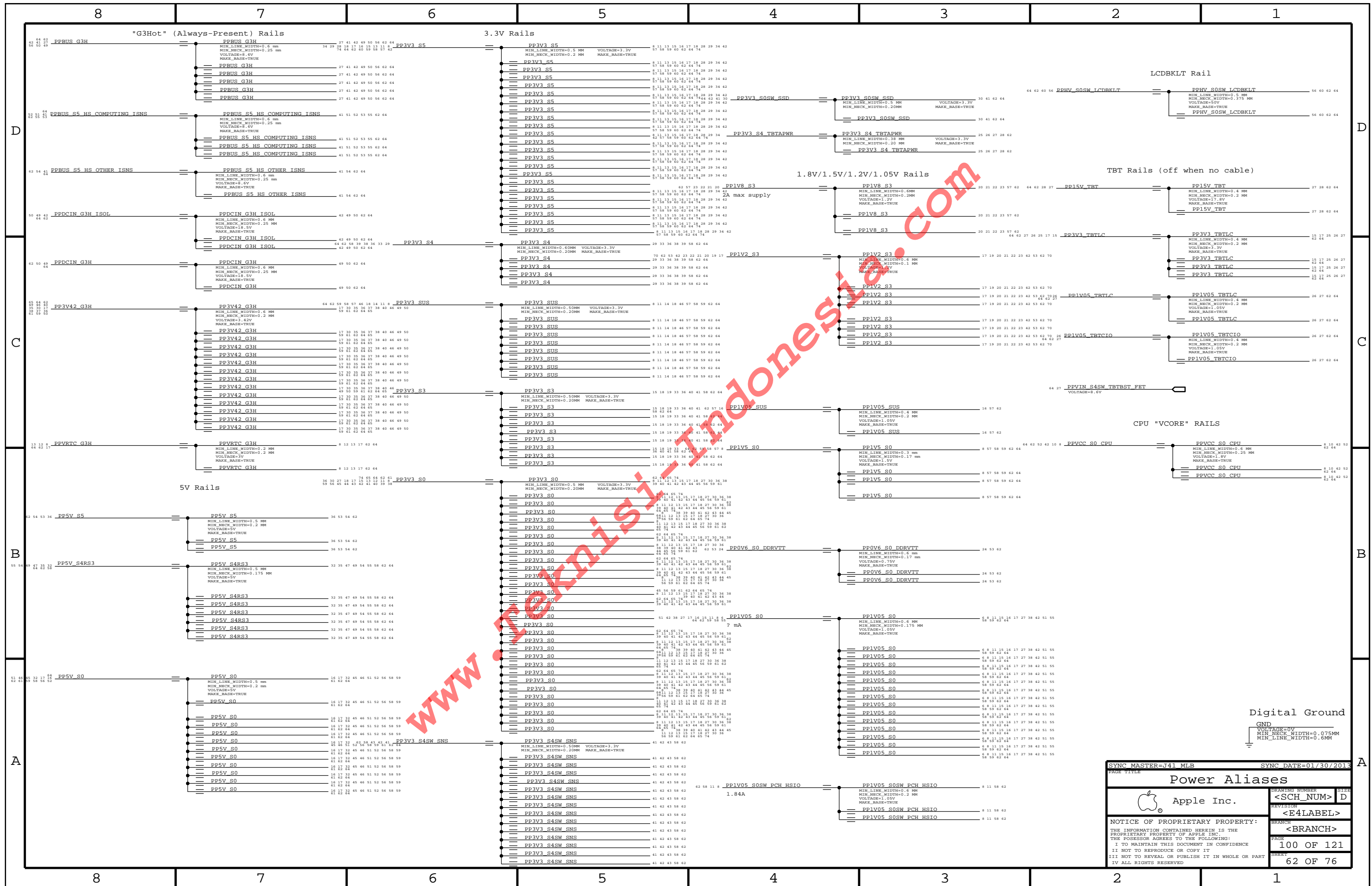




SYNC MASTER=J41 MLB		SYNC DATE=02/06/2013	
PAGE TITLE			
Internal DisplayPort Connector		DRAWING NUMBER	
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		60 OF 76	



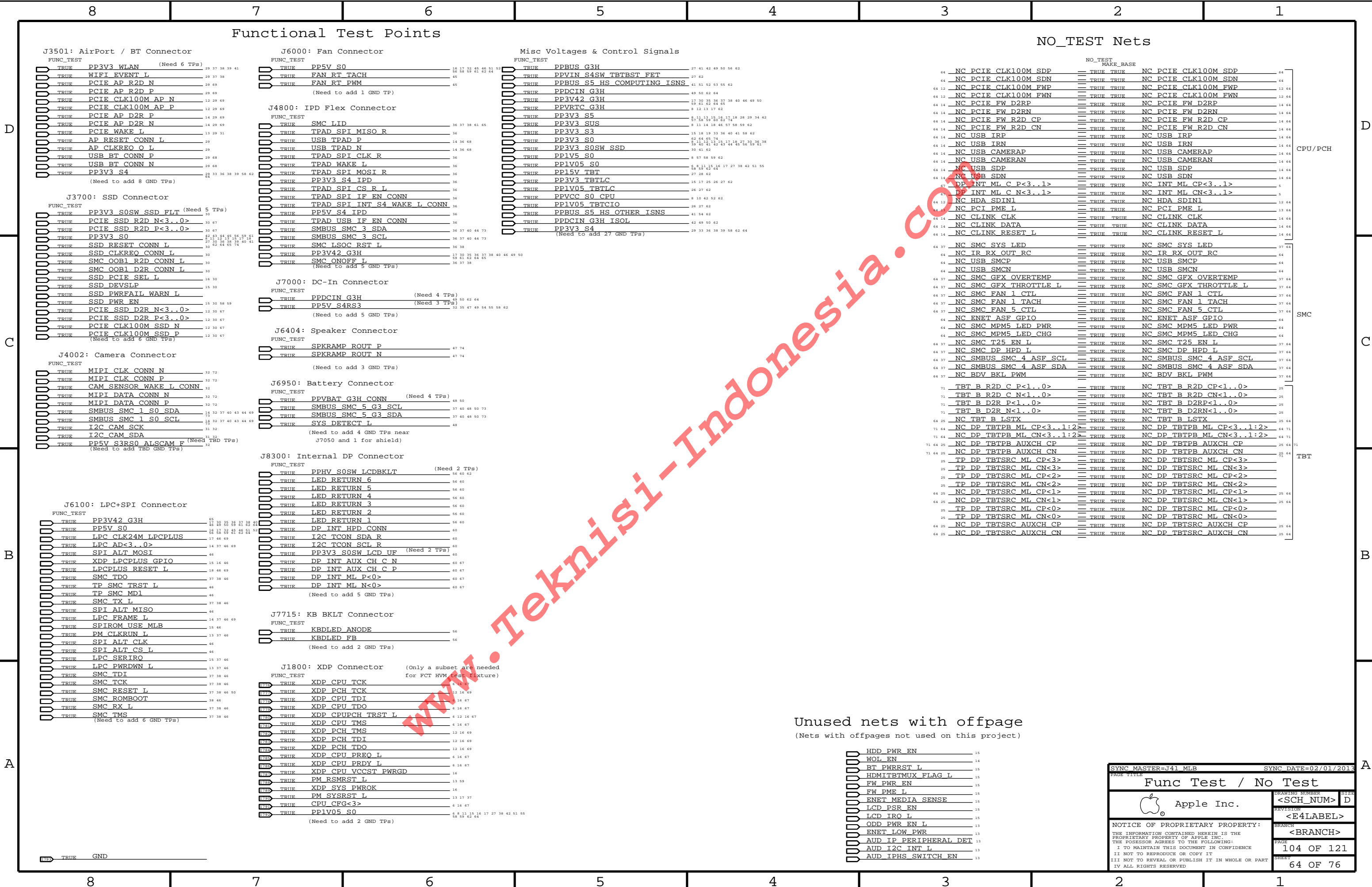
SYNC MASTER=CLEAN J43		SYNC DATE=11/13/2012	
PAGE TITLE			
Left I/O (LIO) Connector			
	Apple Inc.	DRAWING NUMBER	SIZE
		<SCH_NUM>	D
		REVISION	
		<E4LABEL>	
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LPDDR3 Command/Address

Memory Bit/Byte Swizzle

MAKE_BASE				MAKE_BASE					
7	=MEM A A<5>	TRUE	MEM A CAA<0>	20	24	70			
7	=MEM A A<9>	TRUE	MEM A CAA<1>	20	24	70			
7	=MEM A A<6>	TRUE	MEM A CAA<2>	20	24	70			
7	=MEM A A<8>	TRUE	MEM A CAA<3>	20	24	70			
7	=MEM A A<7>	TRUE	MEM A CAA<4>	20	24	70			
7	=MEM A BA<2>	TRUE	MEM A CAA<5>	20	24	70			
70	63	24	20	7	20	24	63	70	
7	=MEM A CAA<6>	TRUE	MEM A CAA<6>	7	20	24	63	70	
7	=MEM A A<11>	TRUE	MEM A CAA<7>	20	24	70			
7	=MEM A A<15>	TRUE	MEM A CAA<8>	20	24	70			
7	=MEM A A<14>	TRUE	MEM A CAA<9>	20	24	70			
7	=MEM A A<13>	TRUE	MEM A CAB<0>	21	24	70			
7	=MEM A CAS L	TRUE	MEM A CAB<1>	21	24	70			
7	=MEM A WE L	TRUE	MEM A CAB<2>	21	24	70			
7	=MEM A RAS L	TRUE	MEM A CAB<3>	21	24	70			
7	=MEM A BA<0>	TRUE	MEM A CAB<4>	21	24	70			
7	=MEM A A<2>	TRUE	MEM A CAB<5>	21	24	70			
70	63	24	21	7	20	24	63	70	
7	=MEM A CAB<6>	TRUE	MEM A CAB<6>	7	20	24	63	70	
7	=MEM A A<10>	TRUE	MEM A CAB<7>	21	24	70			
7	=MEM A A<1>	TRUE	MEM A CAB<8>	21	24	70			
7	=MEM A A<0>	TRUE	MEM A CAB<9>	21	24	70			
70	63	24	21	7	20	21	24	63	70
7	=MEM A ODT<0>	TRUE	MEM A ODT<0>	7	20	21	24	63	70
63	7	TP LPDDR3 RSVD1	TRUE	TP LPDDR3 RSVD1	7	63			
63	7	TP LPDDR3 RSVD2	TRUE	TP LPDDR3 RSVD2	7	63			
7	=MEM B A<5>	TRUE	MEM B CAA<0>	22	24	70			
7	=MEM B A<9>	TRUE	MEM B CAA<1>	22	24	70			
7	=MEM B A<6>	TRUE	MEM B CAA<2>	22	24	70			
7	=MEM B A<8>	TRUE	MEM B CAA<3>	22	24	70			
7	=MEM B A<7>	TRUE	MEM B CAA<4>	22	24	70			
7	=MEM B BA<2>	TRUE	MEM B CAA<5>	22	24	70			
7	=MEM B CAA<6>	TRUE	MEM B CAA<6>	7	22	24	63	70	
7	=MEM B A<11>	TRUE	MEM B CAA<7>	22	24	70			
7	=MEM B A<15>	TRUE	MEM B CAA<8>	22	24	70			
7	=MEM B A<14>	TRUE	MEM B CAA<9>	22	24	70			
7	=MEM B A<13>	TRUE	MEM B CAB<0>	23	24	70			
7	=MEM B CAS L	TRUE	MEM B CAB<1>	23	24	70			
7	=MEM B WE L	TRUE	MEM B CAB<2>	23	24	70			
7	=MEM B RAS L	TRUE	MEM B CAB<3>	23	24	70			
7	=MEM B BA<0>	TRUE	MEM B CAB<4>	23	24	70			
7	=MEM B A<2>	TRUE	MEM B CAB<5>	23	24	70			
70	63	24	23	7	23	24	63	70	
7	=MEM B CAB<6>	TRUE	MEM B CAB<6>	7	23	24	63	70	
7	=MEM B A<10>	TRUE	MEM B CAB<7>	23	24	70			
7	=MEM B A<1>	TRUE	MEM B CAB<8>	23	24	70			
7	=MEM B A<0>	TRUE	MEM B CAB<9>	23	24	70			
70	63	24	23	7	22	23	24	63	70
7	=MEM B ODT<0>	TRUE	MEM B ODT<0>	7	22	23	24	63	70
63	7	TP LPDDR3 RSVD3	TRUE	TP LPDDR3 RSVD3	7	63			
63	7	TP LPDDR3 RSVD4	TRUE	TP LPDDR3 RSVD4	7	63			
7	=MEM A DO<0>	TRUE	MEM A DO<9>	7	70				
7	=MEM A DO<1>	TRUE	MEM A DO<12>	7	70				
7	=MEM A DO<2>	TRUE	MEM A DO<10>	7	70				
7	=MEM A DO<3>	TRUE	MEM A DO<11>	7	70				
7	=MEM A DO<4>	TRUE	MEM A DO<8>	7	70				
7	=MEM A DO<5>	TRUE	MEM A DO<13>	7	70				
7	=MEM A DO<6>	TRUE	MEM A DO<14>	7	70				
7	=MEM A DO<7>	TRUE	MEM A DO<15>	7	70				
7	=MEM A DO<8>	TRUE	MEM A DO<0>	7	70				
7	=MEM A DO<9>	TRUE	MEM A DO<1>	7	70				
7	=MEM A DO<10>	TRUE	MEM A DO<2>	7	70				
7	=MEM A DO<11>								



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	SD Card Aliases																																																																																																																																																																																						
D	<div>J9500: LIO Connector</div> <table> <thead> <tr> <th>FUNC_TEST</th><th></th><th></th><th>MAKE_BASE</th><th></th><th></th></tr> </thead> <tbody> <tr> <td>TRUE PP3V42 G3H</td><td>17</td><td>20</td><td>25</td><td>36</td><td>37 38 40 46 49 50</td></tr> <tr> <td>TRUE PP3V3 S0</td><td>8</td><td>11</td><td>12</td><td>13</td><td>15 16 62 66 74</td></tr> <tr> <td>TRUE PP1V5 S0SW AUDIO</td><td>58</td><td>61</td><td></td><td></td><td>39 40 41 42 43 44 45 56 59 61</td></tr> <tr> <td>TRUE SYS ONEWIRE</td><td>37</td><td>61</td><td></td><td></td><td></td></tr> <tr> <td>TRUE SMC BC ACOK</td><td>37</td><td>38</td><td>50</td><td>61</td><td></td></tr> <tr> <td>TRUE USB PWR EN</td><td>35</td><td>59</td><td>61</td><td></td><td></td></tr> <tr> <td>TRUE SMBUS_SMC_2_S3_SDA</td><td>37</td><td>40</td><td>61</td><td>73</td><td></td></tr> <tr> <td>TRUE SMBUS_SMC_2_S3_SCL</td><td>37</td><td>40</td><td>61</td><td>73</td><td></td></tr> <tr> <td>TRUE SPKRAMP_SHDN_L</td><td>47</td><td>61</td><td></td><td></td><td></td></tr> <tr><td colspan="6"></td></tr> <tr> <td>TRUE FINSTACKSNS_ALERT_L</td><td>39</td><td>61</td><td></td><td></td><td></td></tr> <tr> <td>TRUE SPKRAMP_INNR_N</td><td>47</td><td>61</td><td>74</td><td></td><td></td></tr> <tr> <td>TRUE SPKRAMP_INNR_P</td><td>47</td><td>61</td><td>74</td><td></td><td></td></tr> <tr> <td>TRUE USB_EXTB_N</td><td>14</td><td>61</td><td>68</td><td></td><td></td></tr> <tr> <td>TRUE USB_EXTB_P</td><td>14</td><td>61</td><td>68</td><td></td><td></td></tr> <tr> <td>TRUE PP5V_S0_ALT_AUD_LDO_EN</td><td>61</td><td></td><td></td><td></td><td></td></tr> <tr> <td>TRUE SMC_LID</td><td>36</td><td>37</td><td>38</td><td>61 64</td><td></td></tr> <tr> <td>TRUE HDA_SDOUT</td><td>12</td><td>61</td><td>69</td><td></td><td></td></tr> <tr> <td>TRUE HDA_BIT_CLK</td><td>12</td><td>61</td><td>69</td><td></td><td></td></tr> <tr> <td>TRUE HDA_SDINO</td><td>12</td><td>61</td><td>69</td><td></td><td></td></tr> <tr> <td>TRUE XDP_USB_EXTB_OC_L</td><td>14</td><td>16</td><td>61</td><td></td><td></td></tr> <tr> <td>TRUE HDA_RST_L</td><td>12</td><td>61</td><td>69</td><td></td><td></td></tr> <tr> <td>TRUE HDA_SYNC</td><td>12</td><td>61</td><td>69</td><td></td><td></td></tr> <tr> <td>TRUE USB3_EXTB_D2R_RC_P</td><td>61</td><td>65</td><td>68</td><td></td><td></td></tr> <tr> <td>TRUE USB3_EXTB_D2R_RC_N</td><td>61</td><td>65</td><td>68</td><td></td><td></td></tr> <tr> <td>TRUE USB3_EXTB_R2D_P</td><td>61</td><td>65</td><td>68</td><td></td><td></td></tr> <tr> <td>TRUE USB3_EXTB_R2D_N</td><td>61</td><td>65</td><td>68</td><td></td><td></td></tr> <tr> <td>TRUE AUD_PWR_EN</td><td>13</td><td>59</td><td>61</td><td></td><td></td></tr> </tbody> </table> <div>(Need to add 5 GND TPs)</div>									FUNC_TEST			MAKE_BASE			TRUE PP3V42 G3H	17	20	25	36	37 38 40 46 49 50	TRUE PP3V3 S0	8	11	12	13	15 16 62 66 74	TRUE PP1V5 S0SW AUDIO	58	61			39 40 41 42 43 44 45 56 59 61	TRUE SYS ONEWIRE	37	61				TRUE SMC BC ACOK	37	38	50	61		TRUE USB PWR EN	35	59	61			TRUE SMBUS_SMC_2_S3_SDA	37	40	61	73		TRUE SMBUS_SMC_2_S3_SCL	37	40	61	73		TRUE SPKRAMP_SHDN_L	47	61										TRUE FINSTACKSNS_ALERT_L	39	61				TRUE SPKRAMP_INNR_N	47	61	74			TRUE SPKRAMP_INNR_P	47	61	74			TRUE USB_EXTB_N	14	61	68			TRUE USB_EXTB_P	14	61	68			TRUE PP5V_S0_ALT_AUD_LDO_EN	61					TRUE SMC_LID	36	37	38	61 64		TRUE HDA_SDOUT	12	61	69			TRUE HDA_BIT_CLK	12	61	69			TRUE HDA_SDINO	12	61	69			TRUE XDP_USB_EXTB_OC_L	14	16	61			TRUE HDA_RST_L	12	61	69			TRUE HDA_SYNC	12	61	69			TRUE USB3_EXTB_D2R_RC_P	61	65	68			TRUE USB3_EXTB_D2R_RC_N	61	65	68			TRUE USB3_EXTB_R2D_P	61	65	68			TRUE USB3_EXTB_R2D_N	61	65	68			TRUE AUD_PWR_EN	13	59	61		
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C	<div>Bead Probes</div> <table> <tbody> <tr> <td>68 61 14</td><td>USB3_EXTB_D2R_N</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA511</td></tr> <tr> <td>68 61 14</td><td>USB3_EXTB_D2R_P</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA510</td></tr> <tr> <td>68 65 61</td><td>USB3_EXTB_D2R_RC_N</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA520</td></tr> <tr> <td>68 65 61</td><td>USB3_EXTB_D2R_RC_P</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA521</td></tr> <tr> <td>68 61 14</td><td>USB3_EXTB_R2D_C_N</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA513</td></tr> <tr> <td>68 61 14</td><td>USB3_EXTB_R2D_C_P</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA512</td></tr> <tr> <td>68 65 61</td><td>USB3_EXTB_R2D_N</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA523</td></tr> <tr> <td>68 65 61</td><td>USB3_EXTB_R2D_P</td><td>CTE</td><td>BEAD-PROBE</td><td>BPA522</td></tr> </tbody> </table>									68 61 14	USB3_EXTB_D2R_N	CTE	BEAD-PROBE	BPA511	68 61 14	USB3_EXTB_D2R_P	CTE	BEAD-PROBE	BPA510	68 65 61	USB3_EXTB_D2R_RC_N	CTE	BEAD-PROBE	BPA520	68 65 61	USB3_EXTB_D2R_RC_P	CTE	BEAD-PROBE	BPA521	68 61 14	USB3_EXTB_R2D_C_N	CTE	BEAD-PROBE	BPA513	68 61 14	USB3_EXTB_R2D_C_P	CTE	BEAD-PROBE	BPA512	68 65 61	USB3_EXTB_R2D_N	CTE	BEAD-PROBE	BPA523	68 65 61	USB3_EXTB_R2D_P	CTE	BEAD-PROBE	BPA522																																																																																																																																						
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68 61 14	USB3_EXTB_D2R_P	CTE	BEAD-PROBE	BPA510																																																																																																																																																																																			
68 65 61	USB3_EXTB_D2R_RC_N	CTE	BEAD-PROBE	BPA520																																																																																																																																																																																			
68 65 61	USB3_EXTB_D2R_RC_P	CTE	BEAD-PROBE	BPA521																																																																																																																																																																																			
68 61 14	USB3_EXTB_R2D_C_N	CTE	BEAD-PROBE	BPA513																																																																																																																																																																																			
68 61 14	USB3_EXTB_R2D_C_P	CTE	BEAD-PROBE	BPA512																																																																																																																																																																																			
68 65 61	USB3_EXTB_R2D_N	CTE	BEAD-PROBE	BPA523																																																																																																																																																																																			
68 65 61	USB3_EXTB_R2D_P	CTE	BEAD-PROBE	BPA522																																																																																																																																																																																			
B																																																																																																																																																																																							
A																																																																																																																																																																																							
	8	7	6	5	4	3	2	1																																																																																																																																																																															
							<div> <div>SYNC MASTER=J41 MLB</div> <div>SYNC DATE=09/13/2012</div> </div> <div> <div>Project FCT/NC/Aliases</div> <div>Apple Inc.</div> </div> <div> <div>NOTICE OF PROPRIETARY PROPERTY:</div> <div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.</div> <div>THIS POSSESSOR AGREES TO THE FOLLOWING:</div> <div>I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE</div> <div>II NOT TO REPRODUCE OR COPY IT</div> <div>III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART</div> <div>IV ALL RIGHTS RESERVED</div> </div> <div> <div>DRAWING NUMBER</div> <div><SCH_NUM></div> <div>REVISION</div> <div><E4LABEL></div> <div>BRANCH</div> <div><BRANCH></div> <div>PAGE</div> <div>105 OF 121</div> <div>SHEET</div> <div>65 OF 76</div> </div>																																																																																																																																																																																

	8	7	6	5	4	3	2	1	
D	Functional Test Points								
C	SD Card Aliases								
B	J9500: LIO Connector								
A	<div> <div> <div>FUNC_TEST</div> <div>PP3V42_G3H</div> <div>TRUE</div> <div>17</div> <div>20</div> <div>25</div> <div>36</div> <div>37</div> <div>38</div> <div>40</div> <div>46</div> <div>49</div> <div>50</div> </div> <div> <div>PP3V3_S0</div> <div>TRUE</div> <div>8</div> <div>11</div> <div>12</div> <div>13</div> <div>16</div> <div>62</div> <div>66</div> <div>74</div> </div> <div> <div>PP1V5_S0SW_AUDIO</div> <div>TRUE</div> <div>39</div> <div>40</div> <div>41</div> <div>42</div> <div>43</div> <div>44</div> <div>45</div> <div>56</div> <div>59</div> <div>61</div> </div> <div> <div>SYS_ONEWIRE</div> <div>TRUE</div> <div>37</div> <div>61</div> </div> <div> <div>SMC_BC_ACOK</div> <div>TRUE</div> <div>37</div> <div>38</div> <div>50</div> <div>61</div> </div> <div> <div>USB_PWR_EN</div> <div>TRUE</div> <div>35</div> <div>59</div> <div>61</div> </div> <div> <div>SMBUS_SMC_2_S3_SDA</div> <div>TRUE</div> <div>37</div> <div>40</div> <div>61</div> <div>73</div> </div> <div> <div>SMBUS_SMC_2_S3_SCL</div> <div>TRUE</div> <div>37</div> <div>40</div> <div>61</div> <div>73</div> </div> <div> <div>SPKRAMP_SHDN_L</div> <div>TRUE</div> <div>47</div> <div>61</div> </div> </div> <div> <div>FINSTACKSNS_ALERT_L</div> <div>TRUE</div> <div>39</div> <div>61</div> </div> <div> <div>SPKRAMP_INNR_N</div> <div>TRUE</div> <div>47</div> <div>61</div> <div>74</div> </div> <div> <div>SPKRAMP_INNR_P</div> <div>TRUE</div> <div>47</div> <div>61</div> <div>74</div> </div> <div> <div>USB_EXTB_N</div> <div>TRUE</div> <div>14</div> <div>61</div> <div>68</div> </div> <div> <div>USB_EXTB_P</div> <div>TRUE</div> <div>14</div> <div>61</div> <div>68</div> </div> <div> <div>PP5V_S0_ALT_AUD_LDO_EN</div> <div>TRUE</div> <div>61</div> </div> <div> <div>SMC_LID</div> <div>TRUE</div> <div>36</div> <div>37</div> <div>38</div> <div>61</div> <div>64</div> </div> <div> <div>HDA_SDOUT</div> <div>TRUE</div> <div>12</div> <div>61</div> <div>69</div> </div> <div> <div>HDA_BIT_CLK</div> <div>TRUE</div> <div>12</div> <div>61</div> <div>69</div> </div> <div> <div>HDA_SDINO</div> <div>TRUE</div> <div>12</div> <div>61</div> <div>69</div> </div> <div> <div>XDP_USB_EXTB_OC_L</div> <div>TRUE</div> <div>14</div> <div>16</div> <div>61</div> </div> <div> <div>HDA_RST_L</div> <div>TRUE</div> <div>12</div> <div>61</div> <div>69</div> </div> <div> <div>HDA_SYNC</div> <div>TRUE</div> <div>12</div> <div>61</div> <div>69</div> </div> <div> <div>USB3_EXTB_D2R_RC_P</div> <div>TRUE</div> <div>61</div> <div>65</div> <div>68</div> </div> <div> <div>USB3_EXTB_D2R_RC_N</div> <div>TRUE</div> <div>61</div> <div>65</div> <div>68</div> </div> <div> <div>USB3_EXTB_R2D_P</div> <div>TRUE</div> <div>61</div> <div>65</div> <div>68</div> </div> <div> <div>USB3_EXTB_R2D_N</div> <div>TRUE</div> <div>61</div> <div>65</div> <div>68</div> </div> <div> <div>AUD_PWR_EN</div> <div>TRUE</div> <div>13</div> <div>59</div> <div>61</div> </div>								

MAKE_BASE

TRUE

14

34

65

68

USB3_SD_D2R_P

TRUE

14

34

65

68

USB3_SD_D2R_N

TRUE

14

34

65

68

USB3_SD_R2D_C_P

TRUE

14

34

65

68

USB3_SD_R2D_C_N

TRUE

14

34

65

68

PP3V3_S0SW_SD

PP3V3_S0SW_SD

(MAKE_BASE=TRUE on page 45)

(Need to add 5 GND TPs)

									Bead Probes								
	68 61 14 USB3_EXTB_D2R_N CTE BEAD-PROBE BPA511 68 61 14 USB3_EXTB_D2R_P CTE BEAD-PROBE BPA510 68 65 61 USB3_EXTB_D2R_RC_N CTE BEAD-PROBE BPA520 68 65 61 USB3_EXTB_D2R_RC_P CTE BEAD-PROBE BPA521 68 61 14 USB3_EXTB_R2D_C_N CTE BEAD-PROBE BPA513 68 61 14 USB3_EXTB_R2D_C_P CTE BEAD-PROBE BPA512 68 65 61 USB3_EXTB_R2D_N CTE BEAD-PROBE BPA523 68 65 61 USB3_EXTB_R2D_P CTE BEAD-PROBE BPA522																
	SYNC_MASTER=J41_MLB SYNC_DATE=09/13/2012 PAGE_TITLE Project_FCT/NC/Aliases Apple Inc. <SCH_NUM> <E4LABEL> NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THIS POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED BRANCH <BRANCH> PAGE 105 OF 121 SHEET 65 OF 76																
	8	7	6	5	4	3	2	1									
[illegible][illegible][illegible]

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_S
CPU_8MIL	*	*	CPU_8MIL_2AN

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_COMP	CPU_COMP	*	CPU_COMP_2SE
CPU_COMP	*	*	CPU_COMP_2OTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_20THER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SE
CPU_VCCSENSE	*	*	CPU_VCCSENSE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SECTION
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SE
CLK_PCIE	*	*	CLK_PCIE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP, BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP, BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHER
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHER
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERH
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERH
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERH
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERH
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX20THERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX20THERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	= 2.5x_DIELECTRIC	?
PCIE_RX2RX	*	= 2.5x_DIELECTRIC	?
PCIE_TX20THERTX	*	= 4x_DIELECTRIC	?
PCIE_RX20THERRX	*	= 4x_DIELECTRIC	?
PCIE_TX2TX	*	= 6x_DIELECTRIC	?
PCIE_RX2TX	*	= 6x_DIELECTRIC	?
PCIE_20THERHS	*	= 4x_DIELECTRIC	?
PCIE_20THER	*	= 3x_DIELECTRIC	?

PCH PCIE Spacing			
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHER
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHER
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_20THERH
PCIE_PCH_RX	*_TX	*	PCIE_20THERH
PCIE_PCH_TX	*_RX	*	PCIE_20THERH
PCIE_PCH_RX	*_RX	*	PCIE_20THERH
PCIE_PCH_TX	*	*	PCIE_20THER
PCIE_PCH_RX	*	*	PCIE_20THER


Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL	NET_TYPE	SPACING	
	CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	4 38
	PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
	PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
		CPU_45S	CPU_ITP	XDP_DBRESET_L	16 17
		CPU_45S	CPU_ITP	XDP_CPU_PRRY_L	6 16 64
		CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 16 64
		CPU_27P4S	CPU_COMP	EDP_COMP	
		CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
	CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
		CPU_45S	CPU_ITP	CPU_CFG<15..0>	6 16 64
	CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 37
		CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
	CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	
	CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 37 38 51
	PM_THRMTRIP_T	CPU_45S	CPU_AGTL	PM_THRMTRIP_L	15 38
	DMT_CLK100M	CLK_PCTE_80D	CLK_PCTE	DMT_CLK100M_CPU_P	
	DMT_CLK100M	CLK_PCTE_80D	CLK_PCTE	DMT_CLK100M_CPU_N	
	DPILL_REF_CLK120M	CLK_PCTE_80D	CLK_PCTE	DPILL_REF_CLKP	
	DPILL_REF_CLK120M	CLK_PCTE_80D	CLK_PCTE	DPILL_REF_CLKN	
	ITEPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITEPCPU_CLK100M_P	
	ITEPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITEPCPU_CLK100M_N	
	ITEPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPXDPE_CLK100M_P	
	ITEPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	ITPXDPE_CLK100M_N	
	ITEPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	XDP_CPU_CLK100M_P	
	ITEPCPU_CLK100M	CLK_PCTE_80D	CLK_PCTE	XDP_CPU_CLK100M_N	
	XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16 64
	XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 16 64
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16 64
	XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 16 64
	XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUCH_TRST_L	6 12 16 64
	XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
		CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
		CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	
		CPU_45S	CPU_ITP	CPU_CFG<15..12>	6 16
	(FSR_CPUREST_L)	CPU_45S	CPU_ITP	XDP_CPUREST_L	16
	CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 51
	CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	8 51
	CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
	CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
	CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
	CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
	CPU_VDDO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P	
	CPU_VDDO_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N	
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
	CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
	CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 51
	CPU_SVIDSCCLK	CPU_45S	CPU_COMP	CPU_VIDSCCLK	8 51
	CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 51
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
		PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 64
		PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 64
		PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<3..0>	12 30 64
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_P<3..0>	12 30 64
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_N<3..0>	12 30 64
	PCIE_CLK100M_SSD	CLK_PCTE_80D	CLK_PCTE	PCIE_CLK100M_SSD_P	12 30 64
	PCIE_CLK100M_SSD	CLK_PCTE_80D	CLK_PCTE	PCIE_CLK100M_SSD_N	12 30 64
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
		DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
		DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18
	DP_TBT_MI	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
	DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
		DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18
		DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18
	DP_INT_MI	DP_80D	DP_TX	DP_INT_ML_P<3..0>	60 64
	DP_INT_MI	DP_80D	DP_TX	DP_INT_ML_N<3..0>	60 64
		DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 60 64
		DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 60 64
	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	60 64
	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	60 64
	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 60
	DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 60
		DP_80D	DP_AUX	DP_INT_AUXCH_P	
		DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

SYNC MASTER=CONSTRAINTS		SYNC DATE=09/25/2012	
PART TITLE			
CPU Constraints			
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		REVISION <E4LABEL>	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_QQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_QQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_QQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_QQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_QQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_QQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_QQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_QQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_QQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_QQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_QQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_QQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_QQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_QQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_QQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_QQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_QQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties


ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM A CLK N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM A CLK N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM A ODT<0>	7 20 21 24 63
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM A CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM A CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM A CAA<9..0>	7 20 24 63
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM A CAB<9..0>	7 21 24 63
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM A DQ<7..0>	7 63
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM A DQ<15..8>	7 63
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM A DQ<23..16>	7 63
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM A DQ<31..24>	7 63
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM A DQ<39..32>	7 21 63
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM A DQ<47..40>	7 63
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM A DQ<55..48>	7 63
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM A DQ<63..56>	7 63
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS P<0>	7 63
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM A DQS N<0>	7 63
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS P<1>	7 63
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM A DQS N<1>	7 63
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS P<2>	7 63
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM A DQS N<2>	7 63
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS P<3>	7 63
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM A DQS N<3>	7 63
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS P<4>	7 63
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM A DQS N<4>	7 63
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS P<5>	7 63
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM A DQS N<5>	7 63
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS P<6>	7 21 63
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM A DQS N<6>	7 21 63
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS P<7>	7 63
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM A DQS N<7>	7 63
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM B CLK N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM B CLK N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM B ODT<0>	7 22 23 24 63
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM B CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM B CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM B CAA<9..0>	7 22 24 63
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM B CAB<9..0>	7 23 24 63
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM B DQ<7..0>	7 63
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM B DQ<15..8>	7 63
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM B DQ<23..16>	7 63
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM B DQ<31..24>	7 63
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM B DQ<39..32>	7 23 63
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM B DQ<47..40>	7 63
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM B DQ<55..48>	7 63
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM B DQ<63..56>	7 63
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS P<0>	7 63
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM B DQS N<0>	7 63
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS P<1>	7 63
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM B DQS N<1>	7 63
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS P<2>	7 63
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM B DQS N<2>	7 63
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS P<3>	7 63
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM B DQS N<3>	7 63
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS P<4>	7 63
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM B DQS N<4>	7 63
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS P<5>	7 63
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM B DQS N<5>	7 63
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS P<6>	7 23 63
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM B DQS N<6>	7 23 63
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS P<7>	7 63
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM B DQS N<7>	7 63
		MEM_PWR	PP1V2_S3	17 19 20 21 22 23 42
		MEM_PWR	PP0V6_S3 MEM VREFCA A	18 19 20 21
		MEM_PWR	PP0V6_S3 MEM VREFDO A	18 19 20 21
		MEM_PWR	PP0V6_S3 MEM VREFCA B	18 19 22 23
		MEM_PWR	PP0V6_S3 MEM VREFDO B	18 19 22 23

SYNC_MASTER=CONSTRAINTS

SYNC_DATE=09/25/2012

PAGE TITLE

Memory Constraints



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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_20THER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_20THER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_20THER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_20THER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_20THERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_20THERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_20THER
S2_MEM_DQS*	*	*	S2MEM_20THER
S2_MEM_CMD	*	*	S2MEM_20THER
S2_MEM_CTRL	*	*	S2MEM_20THER
S2_MEM_CLK	*	*	S2MEM_20THER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_20THERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

NET TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 31 32
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 31 32
S2_MEM_CNTRL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 32 64
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 32 64
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 32 64
S2_MEM_PWR		S2_MEM_PWR	PP1V35_CAM 31 32
S2_MEM_PWR		S2_MEM_PWR	PP0V675_CAM_VREF 31 32
S2_MEM_PWR		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 32
S2_MEM_PWR		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 32



PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SENSE_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SENSE_1T01_P2MM	*	=1T01_DIFFPAIR	0.200 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR
THERM_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SPKR_DIFFPAIR	*	=1T01_DIFFPAIR	0.300 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND	*	=STANDARD	?


SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

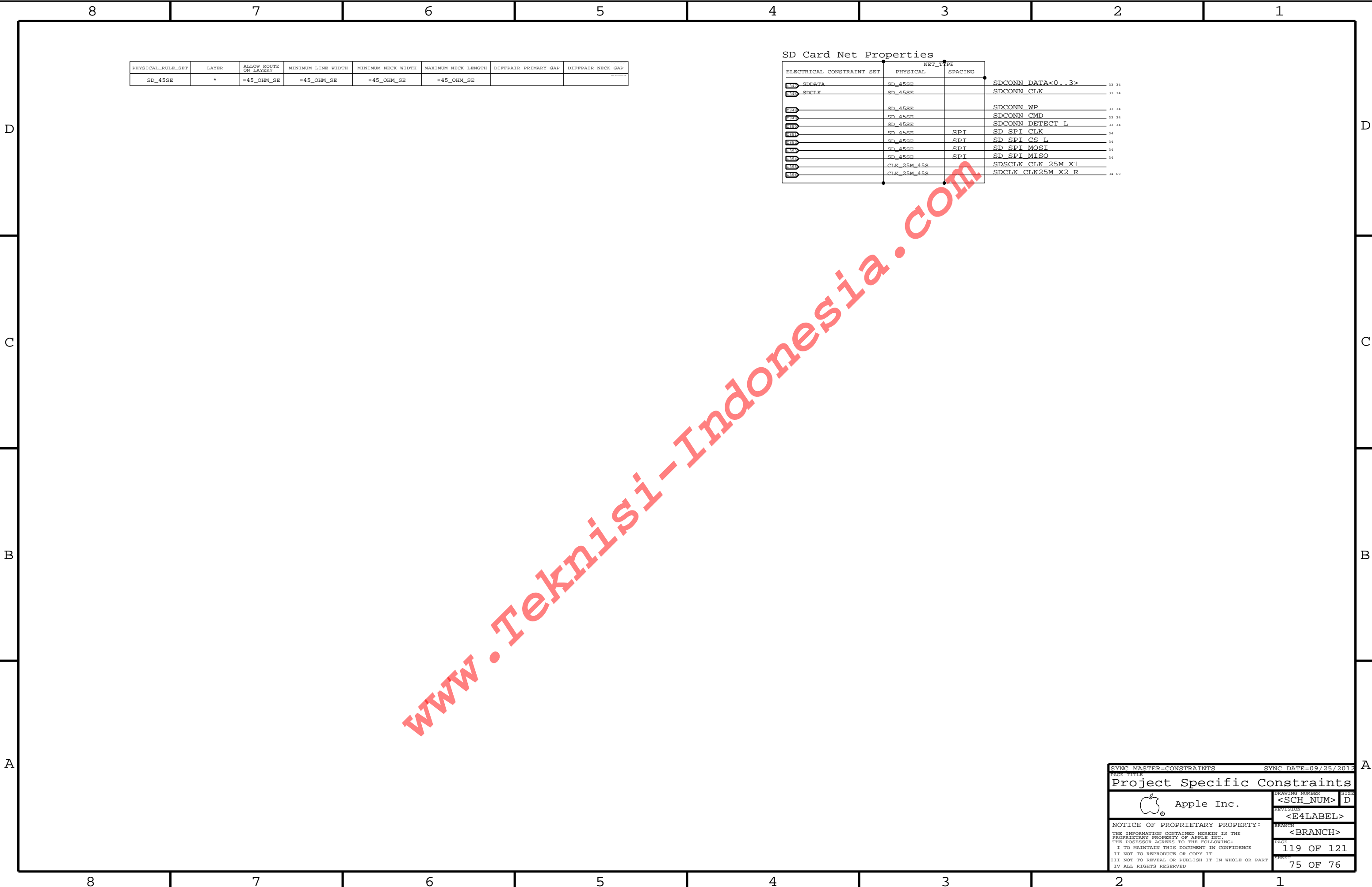
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	INLET THMSNS D1 N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 R N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBTTHMSNS D2 N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	TBT MLBBOT THMSNS N
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	MLBBOT THMSNS D3 P
SENSE_DIFFPAIR	THERM_1T01_45S	THERM	MLBBOT THMSNS D3 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	TBDTHMSNS D2 P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	TBDTHMSNS D2 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THMSNS D2 P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPU THMSNS D2 N
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS N
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVCCIOS0 CS P
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 P
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	CPUVR ISNS1 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISNS2 P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	CPUVR ISNS2 N
SENSE_1T01_P2MM	SENSE		CPUVR ISNS1 P R
SENSE_1T01_P2MM	SENSE		CPUVR ISNS1 N R
SENSE_1T01_45S	SENSE		CPUVR ISUM R P
SENSE_1T01_45S	SENSE		CPUVR ISUM R N
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS CPUDDR P
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS CPUDDR N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3S5 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3S5 P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3 S0 P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 3V3 S0 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS CAMERA P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS CAMERA N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3 S0 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS P3V3 S0 P
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS 1V05 S0 P
SENSE_DIFFPAIR	SENSE_1T01_P2MM	SENSE	ISNS 1V05 S0 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS BMON GAIN P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS BMON GAIN N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS COMPUTING P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS OTHER P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V2 S3 N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS 1V2 S3 P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS AIRPORT P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS SSD P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS LCDBKLT P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS PANEL N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS PANEL P
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS GAIN N
SENSE_DIFFPAIR	SENSE_1T01_45S	SENSE	ISNS HS GAIN P
AUD DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR P
AUD DIFF	1T01_DIFFPAIR	AUDIO	SPKRAMP INR N
1T01_DIFFPAIR	AUDIO		MAX98300 R P
1T01_DIFFPAIR	AUDIO		MAX98300 R N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP ROUT N
	SB_POWER		PP3V3 S5
	SB_POWER		PP3V3 S0
	GND		GND

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE		

SD Card Net Properties


ELECTRICAL_CONSTRAINT_SET	NET TYPE			
	PHYSICAL	SPACING		
R114 SDDATA	SD_45SE		SDCONN DATA<0..3>	33 34
R115 SDCLK	SD_45SE		SDCONN CLK	33 34
R116	SD_45SE		SDCONN WP	33 34
R117	SD_45SE		SDCONN CMD	33 34
R118	SD_45SE		SDCONN DETECT L	33 34
R119	SD_45SE	SPT	SD SPI CLK	34
R120	SD_45SE	SPT	SD SPI CS L	34
R121	SD_45SE	SPT	SD SPI MOSI	34
R122	SD_45SE	SPT	SD SPI MISO	34
R123	CLK_25M_45S		SDCLK CLK 25M X1	34 69
R124	CLK_25M_45S		SDCLK CLK25M X2 R	34 69

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